

# GRID CODE CERTIFICATION BY SIMULATION

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**Keywords:** RENEWABLE ENERGY, GRID CODE, SIMULATION, FAULT-RIDE-THROUGH, HARDWARE-IN-THE-LOOP

## Abstract

To achieve a sustainable energy future, increasing amounts of renewable energy sources (RESs) are being integrated into power systems, replacing traditional high-inertia synchronous generators. Most RES units are inverter-interfaced, lacking natural inertia, which alters power system dynamics, making them more sensitive and dependent on the inverter control schemes. To mitigate stability risks, such as unnecessary disconnections of distributed energy resources during disturbances or faults, grid code requirements and interconnection standards, such as EN50549-1 and EN50549-2 define different operation requirements. These requirements include fault-ride-through (FRT) capability in terms of voltage, frequency, and rate-of-change of frequency, reactive, and negative sequence fault current injection principles during unbalanced faults. Current grid code certification and on-site commissioning tests are costly, time consuming, and limited in scope. This paper proposes simulation-based testing using MATLAB Simulink and hardware-in-the-loop (HIL) platform to efficiently demonstrate grid code compliance. By simulating FRT scenarios, such as under-voltage and over-voltage ride-through, the method provides a cost-effective alternative, reducing time-to-market for manufacturers while maintaining reliability. The simulation results confirm compliance with EN50549 standards, and the HIL testing validates the effectiveness of the approach. This work advances testing procedures, bridge design, and commissioning phases to establish standardized, efficient, and reliable grid code compliance methods.

## 1 Introduction

Recently, serious environmental concerns have arisen due to the intensive use of oil and gases based on fossil fuels [1]. In response, there has been a notable shift towards renewable energy and power inverter systems. Renewable energy, often referred to as clean energy, is based on natural resources, making it more environmentally friendly by reducing carbon emissions from fossil fuel combustion. Therefore, the use of renewable energy resources (RESs) has increased significantly, especially solar photovoltaic (PV) and wind generation [2]. According to the International Energy Agency (IEA), Fig. 1 shows that the global installation capacity of wind turbines has increased from 403 GW to 836 GW between 2015 and 2022, respectively [3], while solar energy installations increased from 228.92 GW to 1,053.12 GW in the same period [4]. RESs, such as solar and wind, depend on natural conditions that fluctuate with weather patterns. Solar energy efficiency, for example, varies depending on the time of day and cloud cover, creating uncertainty that can lead to grid instability [4]. Controlling RESs before integration into the grid is a key challenge [5].

In addition, as the scale of RES installations increases, this variability will increasingly affect the reliability of the electrical grid [6]. An increasing number of inverter interfaces supplied by RES units in the power system replaced many traditional synchronous generators, significantly reducing the inertia of the power system. Most of the new RES-based units are inverter-interfaced without natural inertia, and therefore the dynamics of the future power systems are also different, i.e. more sensitive and dependent on the actual control schemes of

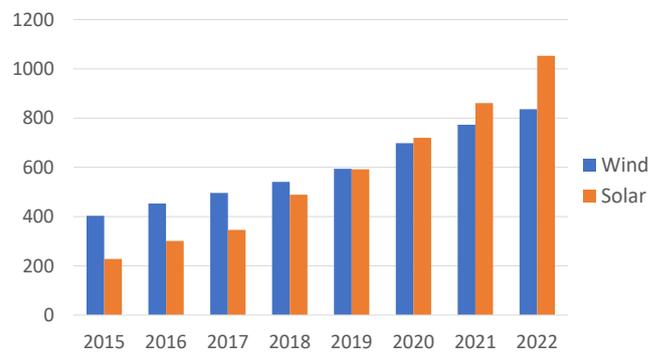


Fig. 1. Installed capacity of solar PV and wind power in GW

the inverter-interfaces. With the increasing integration of RESs into distributed generation [7] as in Fig. 2, concerns about grid stability have led to the development of standards and grid codes both at the national and international level. These codes are continuously updated to accommodate the growing share of inverter-based energy, ensuring the resilience of the grid and optimizing the extraction of renewable energy [8]. The main challenge of RESs integrated into the grid is to ensure their compliance with the requirements of the grid code. This is essential because RESs have a significant impact on the overall reliability of the network. To ensure the stability of the electrical system, it is necessary to test the compatibility of these sources before integration. Grid code compliance testing is an essential process to verify that RES-based inverters

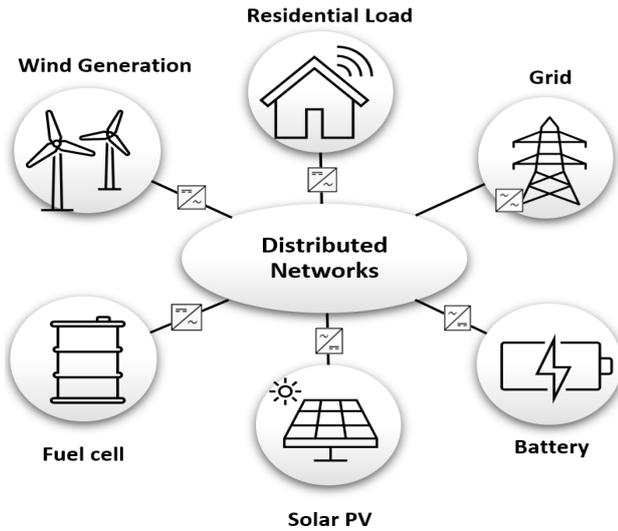


Fig. 2. Distribution network supplied by RES-based inverter.

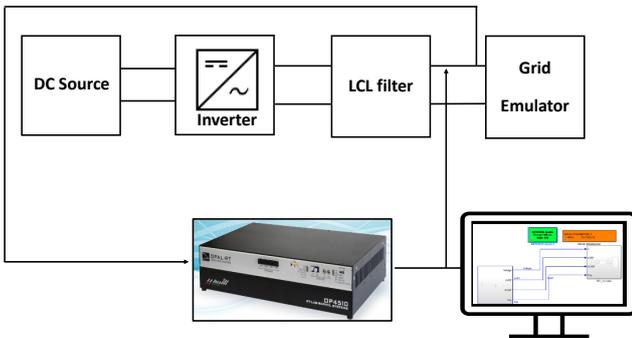


Fig. 3 A laboratory setup for inverter certification by simulation.

meet the required standards. However, traditional on-site testing methods are resource-intensive and time-consuming and require extensive planning and financial resources. These tests involve coordinating with various stakeholders and substantial physical infrastructure. Fig. 3 shows the laboratory setup for the grid code certification by simulation platform, where the inverter is placed as the device under test. Simulation-based compliance testing presents a safer and more efficient alternative. The simulation is able to mimic the events created in the on-site testing. It can simulate real-life grid conditions and fault scenarios at the point of the grid-connected inverter similar to the actual grid performance. This approach minimizes the risk of equipment damage during testing while offering a more cost-effective solution. Furthermore, simulation-based testing accelerates the certification process, reduces the need for extensive physical tests, and reduces associated costs for industrial manufacturers. In addition, it improves the reliability of the product by allowing the early detection and correction of potential compliance issues, making the certification process more efficient and effective [8], [9]. This shift toward simulation-based compliance can significantly contribute to the broader

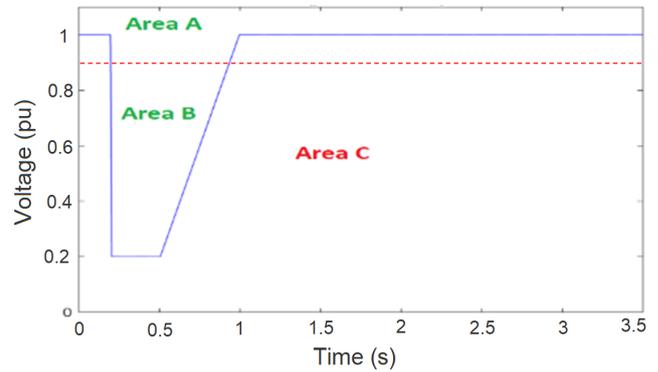


Fig. 4. UVRT voltage - time curve.

adoption and integration of renewable energy into existing grids.

The purpose of this paper is to develop a simulation model that can be applied when testing the grid code compliance of an inverter using MATLAB Simulink. The objective is to evaluate different scenarios of undervoltage ride-through (UVRT) and overvoltage ride-through (OVRT) capabilities of a grid-connected inverter using simulation. This simulation model is the first version for future HIL-based testing using the OPAL-RT real-time simulator. The EN 50549-1, EN 50549-2 and EN 50549-10 Europe standards for grid connected generation plants are utilized as a basis when developing this model; the first two standards specify the required functionalities for the test, while the third one offers instructions on how the tests should be performed. Different OVRT and UVRT events have been implemented in the model to test compliance with the EN50549-1 standard. The thresholds for the UVRT and OVRT requirements have been predefined in the MATLAB script according to the standard.

## 2 Grid Codes

### 2.1 Under Voltage Ride Through (UVRT)

UVRT capability allows generating modules to remain connected during low voltage and fault conditions in distributed networks [10]. Solar PV and wind turbines face challenges during faults, leading to widespread voltage dips. These dips can cause disconnections from the grid, resulting in power outages and instability. To mitigate this, generating units must have the capability of UVRT according to the grid code requirements. For PV systems, this means continued connection during voltage fluctuations, and provision of reactive power to improve the voltage of the grid [11]. Wind turbines should also have UVRT capability and stay connected during voltage sags, helping to maintain grid stability and continuous power generation [12]. UVRT improves grid stability, provides reactive power support, and ensures proper integration of wind turbines [13]. Fig. 4 shows the UVRT voltage-time curve, with Area A is for normal operation, Area B for continued operation during voltage recovery by injecting more reactive power, and Area C for

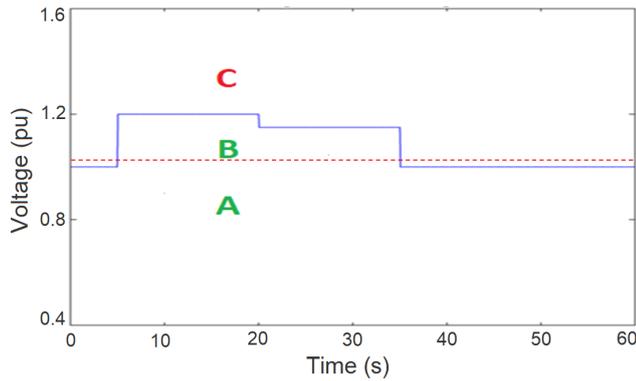


Fig. 5. OVRT voltage - time curve.

disconnection [14]. The curve was created using MATLAB and follows the EN50549-1 standard.

### 2.2 Over Voltage Ride Through (OVRT)

OVRT refers to a generating unit’s capability to remain connected to the grid for a short duration, typically if the voltage increases higher than the nominal voltage. Fig. 5 shows the curve of OVRT capability according to the EN50549-1 standard. Region A represents the condition in which the system operates within the normal condition connected to the grid. Region B shows that the inverter must remain connected to the grid for a short period to support the grid and mitigate the grid voltage. Region C shows that the inverter must be disconnected from the grid when the voltage increases to a level higher than the OVRT threshold [14].

## 3 Simulation Model

The aim of this section is to verify the simulation model for the grid code certification by simulation and to demonstrate the results during the UVRT and OVRT performance. The DC source in Fig. 6 can represent any type of RESs (such as solar power or wind turbines) connected to the grid emulator through a three-phase inverter. The inverter is the device under test connected to the grid through the LCL filter. The main input signal to the UVRT and OVRT simulation block is in p.u. Therefore, a three-phase signal measured from the V-I voltage measurement block is converted to a p.u. for UVRT and OVRT tests. This can be done using the sequence analyzer block, and the p.u. signal is sent to the simulation block of the grid code requirements. A three-phase zero-impedance voltage source emulates the grid, creating UVRT and OVRT events by adjusting the voltage amplitude over time.

The test aims to meet the EN50549-1 and EN50549-2 thresholds. The grid code simulation model from [15] has been adjusted for compliance, comparing the inverter output signal with the UVRT and OVRT thresholds. A Simulink scope with four outputs facilitates the comparison between the voltage signals, thresholds, and trip signals. If the grid voltage is within the UVRT and OVRT thresholds, the trip signal remains at

zero. Once the voltage decreases or exceeds the EN50549 standard thresholds, the trip signal will be activated, that is, switch from 0 to 1, and stay at 1 preventing more triggering.

## 4 Simulation Results

Fig. 7 outlines the essential criteria that must be met to connect the inverter to the grid according to the EN50549-1 standard. Despite the protection interface settings, these criteria must be provided and followed. The graph divided the curve into three zones to facilitate explanation. For all simulation results, the x and y axes represent the time in seconds and the voltage p.u., respectively.

For all results, the grid voltage signal is presented in green, the UVRT threshold is in red, the OVRT is in brown, and the trip signal is in magenta color. The trip signal is only activated (from 0 to 1) if the voltage signal crosses the UVRT thresholds. As the trip signal is activated, this implies that the inverter must be disconnected from the grid. Or, the trip signal remains deactivated at 0, which implies that the inverter should stay connected to the grid. For example, in zone A, the voltage must not decrease below 0.85 p.u. for more than 1.5 seconds.

### 4.1 Under Voltage Ride Through (UVRT) Test

Fig. 8 depicts one of the UVRT scenarios. The simulation starts with a nominal voltage of 1 p.u. for a period of 2 seconds. Then, due to the fault occurrence, the voltage signal has been reduced to 0.84 p.u. for a time less than 1.5 s. This scenario shows the voltage dynamics within zone A where the voltage is still above the UVRT voltage and the time threshold. Therefore, the inverter should be connected to the grid with normal operation. As a result, the trip signal remains deactivated at 0. If the voltage decreased to 0.84 p.u. and continued for a time greater than 1.5 s as in Fig. 9, we can notice that the grid voltage signal crossed the UVRT threshold and therefore the breaker trip signal is activated to 1, which implies that the inverter is allowed to be completely disconnected from the power grid.

When the voltage signal decreased to 0.6 p.u. for more than 1.5 s. As illustrated in Fig. 10, the voltage crossed the UVRT region. Therefore, the grid-connected inverter is disconnected, and the trip signal is activated at the same time that the voltage signal enters the UVRT thresholds.

### 4.2 Over Voltage Ride Through (OVRT) Test

Fig. 11 shows one of the OVRT scenarios. Initially, the voltage of the grid is begin at the nominal value of 1 p.u. for 0.4 seconds. Then, suddenly the voltage increased to 1.23 p.u. for a duration of less than 0.1 seconds. Because the voltage signal has not violated the OVRT threshold, according to the EN50549-1 standard, the inverter should remain connected. Therefore, the trip signal has not been turned on. If the voltage level increases to more than 1.25 p.u., it will cross the OVRT boundary, and the trip signal will immediately be activated.

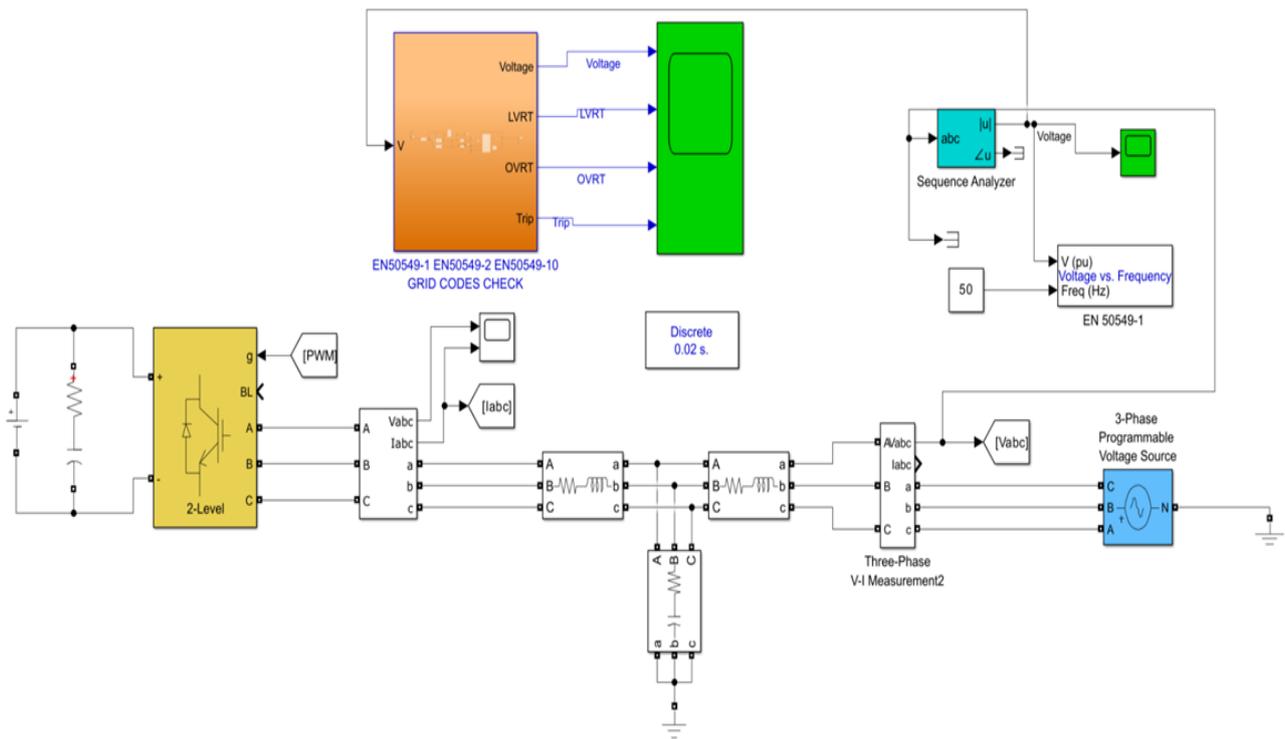


Fig. 6. Simulation-based grid compliance tests.

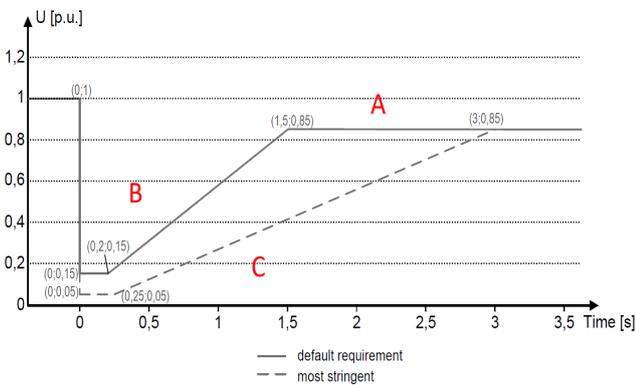


Fig. 7. Under-voltage ride through capability.

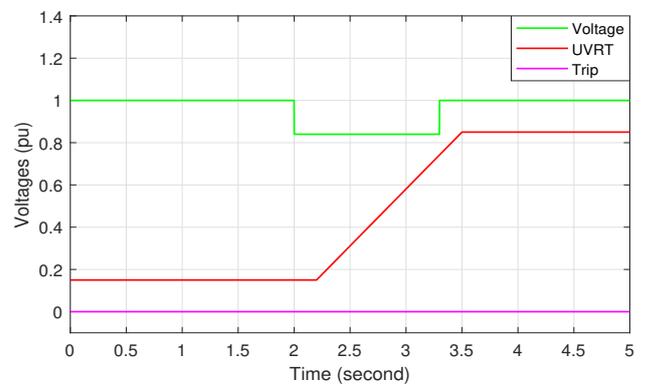


Fig. 8. Voltage dip to 0.84 V (p.u) for time less than 1.5 s.

## 5 Conclusion

This paper presents an easy-to-use simulation model for grid code certification of grid-connected inverters. The model has been designed to match the grid code requirement of the EN50549 Europe standard, particularly for the fault-ride-through capability. The results focused on testing the under-voltage and overvoltage ride-through capability. The goal is to reduce the time to market and onsite testing of the grid-connected inverter by utilizing the certification by simulation. This model will pave the way for developing a complete HIL setup to test inverter grid code requirements by third-party organizations, which will reduce time and cost. It also helps

to increase the competences of the industry sectors energy to renewable energy integration. In the test setup, the inverter output signals are compared with predefined thresholds based on the EN50549-1, EN50549-2, and EN50549-10 standards.

## 6 Acknowledgments

This work was carried out as part of “Smart Grid 2.0” project funded by Business Finland with Grant No. 1386/31/2022.

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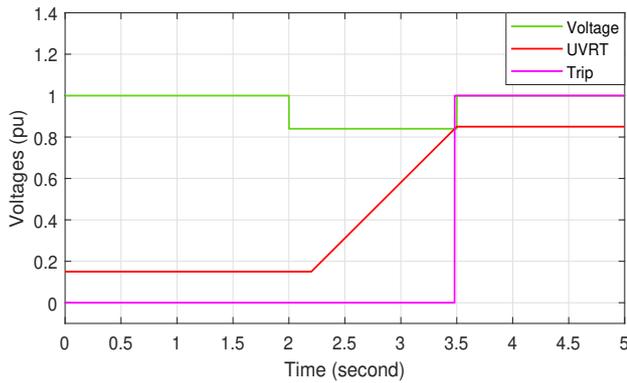


Fig. 9. Voltage dip to 0.84 V (p.u) for time greater than 1.5 s.

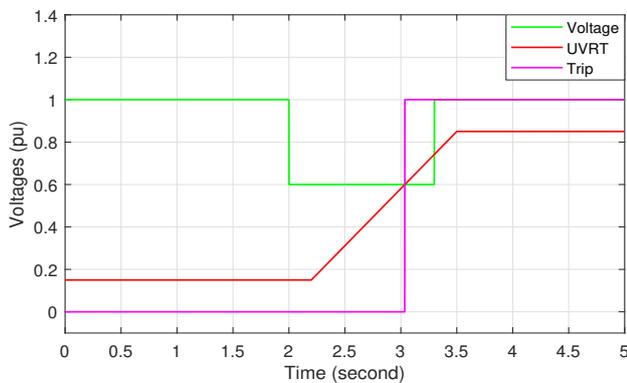


Fig. 10. Voltage dip to 0.6 V (p.u) for time less than 1.5 s.

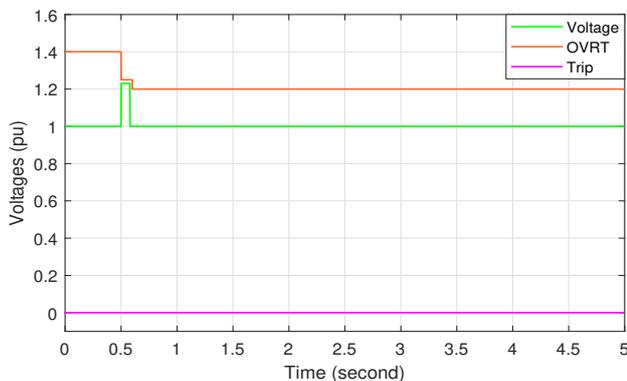


Fig. 11 Voltage increase to 1.23 V (p.u) for time less than 0.4 s.

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