

ORIGINAL ARTICLE

A single-source switched-capacitor-based 25-level sextuple boost inverter with a low switch count

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Abstract

Today, multilevel inverters are widely utilized in various applications. Reducing the number of components in the design of these converters is one of the crucial goals so that they have less volume and cost. This paper presents a single-source structure for a multilevel switched-capacitor inverter with voltage boost capability. The proposed structure can generate 25 sinusoidal-like step voltage levels with a six times amplitude increase compared to the input. This converter uses only one direct current (DC) power source, 14 switches, and four capacitors. The nearest level control switching method has been used to control the converter, create voltage levels, and select the switching modes. A comprehensive comparison has been made with other recently presented structures to demonstrate the efficiency of the proposed structure. The advantages of the proposed structure include using only one DC voltage source, the ability to increase the output voltage six times compared to the input, the use of fewer power electronics components compared to the number of voltage levels, proper efficiency, self-balancing of capacitors, and as a result, the lower cost. The performance accuracy of the proposed converter has been simulated in the MATLAB Simulink environment and then evaluated by a laboratory prototype.

KEYWORDS

multilevel inverter, nearest level switching, power electronics, switched-capacitor

1 | INTRODUCTION

Multilevel inverters are suitable for some applications, such as renewable energy sources, electric vehicles (EVs), transportation, high-frequency power distribution, variable speed drives, and so on. Some of the significant features of these converters are improved power quality, lower voltage stress, lower switching

losses, and, as a result, better efficiency.^{1–3} The task of the voltage source inverter is to convert the direct input voltage into sinusoidal voltage with adjustable frequency and amplitude. Multilevel converters can produce a waveform with better quality and similar to sine through switching and creating a balanced combination of direct current (DC) power supplies or capacitors, which leads to a reduction in harmonic

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distortion and, accordingly, a reduction in the output filter volume.

In general, the most commonly used multilevel inverters are divided into three categories: the first category is Neutral Point Diode Clamped inverters (NPC), the second category is flying capacitor (FC) multilevel inverters, and the third category is cascaded H-bridge multilevel inverters (CHB).^{4–6} In the NPC multilevel inverter, the neutral point voltage is controlled by clamping diodes, through which the voltage levels can be produced. In the FC multilevel inverter, the required output voltage levels are produced by collecting the voltage of the FCs and the DC voltage source. Capacitor voltage imbalance and a large number of components are the main problems of NPC and FC multilevel inverters. Besides, the CHB multilevel inverter needs several independent DC sources, and the number of components is significantly increased to produce higher levels. On the other hand, the voltage gain of these conventional structures is not higher than 1, and these structures cannot produce an output voltage amplitude higher than the input without utilizing transformers or DC–DC converters. In the context of reducing the number of independent DC sources and providing the boost capability in the multilevel inverters, switched-capacitor (SC) based structures have been introduced.⁷

The SC inverters can also increase the output voltage compared to the input. In these converters, the output step voltage is produced from the combination of the voltage of the DC sources and the capacitors by utilizing switching and correct charging and discharging of the capacitors. The SC inverters also have some drawbacks, including capacitor inrush current and a higher number of components. During the charging of the capacitor through the input source, the switches placed in the capacitor charging path must withstand the charging current. Khoun-Jahan⁸ presented a solution to reduce the inrush current, which is attenuated by a limiting inrush current inductor. Anand et al.⁹ have suggested another method for reducing charge current, which is based on a control strategy. This method, known as soft switching or quasicharge, reduces inrush currents through high-frequency switching and controlled charging and discharging. In Wang,¹⁰ a structure is proposed for an SC multilevel inverter. This structure produces a nine-level output voltage using a half-bridge and can increase the output voltage to twice the input voltage. The maximum blocked voltage on four half-bridge switches is $2V_{dc}$. If the structure expands, the voltage stress on the switches will not increase, but the number of input sources and switches will increase. The topologies presented in Babaei and Gowgani¹¹ and

Shalchi Alishah et al.¹² use a similar basic structure that requires less equipment to generate the output voltage levels. The base structure consists of a DC source and a capacitor that can increase the output voltage gain to two times the input voltage. Self-balancing of capacitors voltage is created by charging the capacitor in parallel with the source and discharging it in series with the source. On the other hand, if these structures are generalized to access higher levels, the number of input sources will rise. The structure presented in Saeedian et al.¹³ has a lower total standing voltage (TSV) and requires switches with a lower voltage range. At the same time, it uses two capacitors to generate five-level voltage and has a low voltage gain. In Sun et al.¹⁴ and Khoun Jahan et al.,¹⁵ structures are presented that produce output voltage levels without using an H-bridge module and have the advantage of modularity. These structures have lower voltage stress in the switches, but if extended to higher levels, they require more switches and capacitors. In Anand and Singh,¹⁶ a new structure of SC is introduced. This structure has lower voltage stress and can increase the input voltage up to six times using three SCs. The structure presented in Sathik et al.¹⁷ creates a nine-level output voltage with a voltage gain equal to four using an input source. In this structure, four switches withstand the maximum output voltage. Singh and Mandal¹⁸ proposed a 17-level single-source inverter with a reduced input current spike. The structure is composed of a relatively large number of switches, which leads to voltage division among the switches, resulting in lower voltage stress on each switch. In Ponnusamy et al.,¹⁹ a new structure with two input sources and lower switch power for PV applications has been introduced. This structure has been tested using a closed-loop method, and its dynamic behavior has been evaluated. In Sathik et al.,²⁰ a single-source structure with a continuous input current for photovoltaic applications has been introduced. This topology generates continuous input current through a DC–DC converter and can increase the output voltage to eight times the input voltage. In this structure, the soft charging technique has been employed to reduce inrush currents. Jena²¹ introduced a 13-level structure with a gain factor of six, which consists of 13 switches, four capacitors, and two diodes. This structure is less stressed because only two switches withstand the maximum output voltage. In Jena et al.,²² a seven-level waveform with a boost factor of three is generated by an input power supply, two capacitors, eight switches, and a diode. In reference to Jena et al.,²³ a seven-level topology with less equipment stress is suggested. The main weakness

of this structure is the use of a H-bridge module to produce bipolar voltage levels, which leads to voltage stress increases. Jena et al.²⁴ present a five-level structure that is capable of increasing voltage with a gain factor of two. This structure produces the negative voltage levels without using H-bridge module, resulting a lower voltage stress. In this structure, all of semiconductor devices withstand a voltage equal to the DC source.

This paper presents a single-source structure for an SC multilevel inverter. This structure can produce 25 voltage levels by 14 switches, four capacitors, and only one DC power supply. The advantages of the proposed structure include being a single source, using fewer components compared to the voltage levels, less harmonic distortion that addresses the limitations stated in standards IEEE-1547²⁵ and IEEE-519,²⁶ capacitor voltage self-balancing capability, boost capability of the output voltage up to six times the input voltage, suitable switching losses and the possibility of expanding the structure to more levels. The maximum number of simultaneous conducting switches which are passing the load current is seven switches, which is only half of the switches in the structure. Reducing the number of current conducting switches has led to a reduction in conduction losses and an increase in the efficiency. At the same time, one of the switches is turned on and off with the line frequency, which leads to the reduction of the switching losses of this switch. The proposed converter can work under different power factors, making it a convenient option for industrial applications.

The rest of this paper is configured as follows. The proposed structure is introduced in Section 2; besides the principles of operation, switching modes as well as charging and discharging of capacitors are explained in detail in this section. Next, the design procedure for the capacitors utilized in the proposed structure is presented.

Then the modulation strategy and the expanded structure are also presented in this section. Section 3 evaluates the losses of the proposed converter, and a comparative evaluation is carried out in Section 4. Simulation and laboratory results are presented in Section 5. Finally, a conclusion is made in Section 6.

2 | OPERATION PRINCIPLES OF THE PROPOSED STRUCTURE

The circuit of the proposed 25-level structure is shown in Figure 1. This converter includes 14 switches (S_1 – S_{14}), four capacitors (C_1 – C_4), and a DC power supply. The switches S_5 and S_8 do not contain reverse parallel diodes. An inductor (L_r) paralleled with a diode (D_r) is introduced for soft charging of capacitors. This converter produces $(0, \pm 0.5V_{in}, \pm V_{in}, \pm 1.5V_{in}, \dots, \pm 6V_{in})$ voltage levels using an enhanced H-bridge module. In the negative half-cycle, the output levels of $V_{in}, 2V_{in}, \dots, 6V_{in}$ are generated similarly by turning on the S_{3a} and S_{4a} switches instead of S_{1a} and S_{2a} . In addition, there are two current paths to produce some levels. The voltage of capacitors C_1 and C_2 is stabilized at the V_{dc} . Capacitor C_3 can generate the total voltage produced by the source and C_1 – C_2 capacitors, whose voltage is stabilized at $3V_{dc}$. The capacitor C_4 is charged and discharged symmetrically in positive and negative half-cycles, and its voltage is stabilized at $0.5V_{dc}$ to obtain the boost factor of 5 and 25 voltage levels. The switching states of the proposed inverter are shown in Table 1. Additionally, in Figure 2, the operation states and current paths for the positive half-cycles are presented. Table 2 shows the current stresses of different switches of the proposed topology. In this table, I_o is the output current, and I_c is the charging current. Also, the voltage stress of each switch at different voltage levels is presented in Table 3.

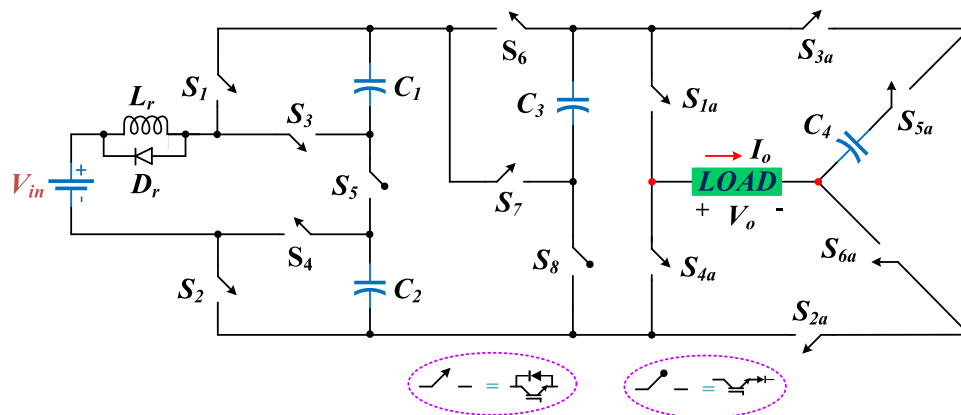


FIGURE 1 The structure of the proposed multilevel inverter.

TABLE 1 Switching modes of the proposed structure.

ON switches for positive half-cycle	Voltage steps	ON switches for negative half-cycle
$S_1-S_4-S_5-S_{2a}-S_{4a}-S_{6a}$	0	$S_1-S_4-S_5-S_{1a}-S_{3a}-S_{6a}$
$S_{5a}-S_{3a}-S_{1a}$	$\pm 0.5V_{dc}$	$S_1-S_2-S_6-S_{3a}-S_{5a}-S_{4a}$
$S_1-S_2-S_6-S_{1a}-S_{6a}-S_{2a}$	$\pm V_{dc}$	$S_1-S_2-S_6-S_{3a}-S_{6a}-S_{4a}$
$S_1-S_2-S_6-S_{1a}-S_{5a}-S_{2a}$	$\pm 1.5V_{dc}$	$S_1-S_4-S_5-S_6-S_{3a}-S_{5a}-S_{4a}$ $S_2-S_3-S_5-S_6-S_{3a}-S_{5a}-S_{4a}$
$S_2-S_3-S_5-S_6-S_{1a}-S_{6a}-S_{2a}$	$\pm 2V_{dc}$	$S_2-S_3-S_5-S_6-S_{3a}-S_{6a}-S_{4a}$
$S_1-S_4-S_5-S_6-S_{1a}-S_{6a}-S_{2a}$		$S_2-S_3-S_5-S_6-S_{3a}-S_{6a}-S_{4a}$
$S_1-S_4-S_5-S_6-S_{1a}-S_{5a}-S_{2a}$	$\pm 2.5V_{dc}$	$S_3-S_4-S_6-S_8-S_{3a}-S_{5a}-S_{4a}$
$S_2-S_3-S_5-S_6-S_{1a}-S_{5a}-S_{2a}$	$\pm 3V_{dc}$	$S_3-S_4-S_6-S_8-S_{3a}-S_{6a}-S_{4a}$
$S_3-S_4-S_6-S_8-S_{1a}-S_{6a}-S_{2a}$		
$S_3-S_4-S_6-S_8-S_{1a}-S_{5a}-S_{2a}$	$\pm 3.5V_{dc}$	$S_1-S_2-S_7-S_{3a}-S_{5a}-S_{4a}$
$S_1-S_2-S_7-S_{1a}-S_{6a}-S_{2a}$	$\pm 4V_{dc}$	$S_1-S_2-S_7-S_{3a}-S_{6a}-S_{4a}$
$S_1-S_2-S_7-S_{1a}-S_{5a}-S_{2a}$	$\pm 4.5V_{dc}$	$S_1-S_4-S_5-S_7-S_{3a}-S_{5a}-S_{4a}$ $S_2-S_3-S_5-S_7-S_{3a}-S_{5a}-S_{4a}$
$S_2-S_3-S_5-S_7-S_{1a}-S_{6a}-S_{2a}$	$\pm 5V_{dc}$	$S_2-S_3-S_5-S_7-S_{3a}-S_{6a}-S_{4a}$
$S_1-S_4-S_5-S_7-S_{1a}-S_{6a}-S_{2a}$		$S_1-S_4-S_5-S_7-S_{3a}-S_{6a}-S_{4a}$
$S_1-S_4-S_5-S_7-S_{1a}-S_{5a}-S_{2a}$	$\pm 5.5V_{dc}$	$S_3-S_4-S_7-S_{3a}-S_{5a}-S_{4a}$
$S_2-S_3-S_5-S_7-S_{1a}-S_{5a}-S_{2a}$		
$S_3-S_4-S_7-S_{1a}-S_{6a}-S_{2a}$	$\pm 6V_{dc}$	$S_3-S_4-S_7-S_{3a}-S_{6a}-S_{4a}$

2.1 | Self-balancing of capacitors voltage and their capacity determination

Figure 3 displays the charging and discharging pattern of each capacitor in a 25-level output voltage period. According to this figure, after a period of discharge, each capacitor needs less time to charge and recovers quickly. Sufficient charging of capacitors and low parasitic resistance lead to appropriate voltage balance of capacitors. The capacitor C_4 is discharged in the positive half-cycle and charged in the negative half-cycle with the same pattern so that its voltage is maintained at half the value of the input source. Obtaining the discharge time of capacitors and the largest discharging period is essential in choosing the most appropriate value of capacitor capacity.²⁷ Further, the rated frequency and the value of the impedance of the output load affect the voltage ripple and the capacity of the capacitors. The amount of discharge for the capacitors C_1 to C_4 is obtained through (1)–(4), respectively. In these relations, I_o is the amplitude of the output current, and φ is the

phase angle of the load impedance, which is the phase difference between the output voltage and the load current.

$$\Delta Q_{C_1} = 2 \int_{t_0}^{T/4} I_o \sin(\omega t - \varphi) dt, \quad (1)$$

$$\Delta Q_{C_2} = 2 \int_{t_1}^{T/4} I_o \sin(\omega t - \varphi) dt, \quad (2)$$

$$\Delta Q_{C_3} = 2 \int_{t_7}^{T/4} I_o \sin(\omega t - \varphi) dt, \quad (3)$$

$$\begin{aligned} \Delta Q_{C_4} = & \int_{t_1}^{t_2} I_o \sin(\omega t - \varphi) dt + \int_{t_3}^{t_4} I_o \sin(\omega t - \varphi) \\ & dt + \int_{t_5}^{t_6} I_o \sin(\omega t - \varphi) dt \\ & + \int_{t_7}^{t_8} I_o \sin(\omega t - \varphi) dt \\ & + \int_{t_9}^{t_{10}} I_o \sin(\omega t - \varphi) dt \\ & + \int_{t_{11}}^{t_{12}} I_o \sin(\omega t - \varphi) dt. \end{aligned} \quad (4)$$

Considering that the output voltage pattern in Figure 3 is based on the fundamental frequency switching scheme, half period of $T/2$ can be divided into 24 time intervals (t_1 – t_{24}). Therefore, the relations presented in (6) can be calculated through the general Equation (5).²⁸ In this regard, N_1 is the number of output voltage levels.

$$t_i = \frac{\sin^{-1}\left(\frac{2i-1}{N_1-1}\right)}{\omega}, \quad (5)$$

$$\begin{aligned} t_1 &= \frac{\sin^{-1}(1/24)}{\omega}, \quad t_2 = \frac{\sin^{-1}(3/24)}{\omega}, \quad t_3 = \frac{\sin^{-1}(5/24)}{\omega}, \\ t_4 &= \frac{\sin^{-1}(7/24)}{\omega}, \quad t_5 = \frac{\sin^{-1}(9/24)}{\omega}, \quad t_6 = \frac{\sin^{-1}(11/24)}{\omega}, \\ t_7 &= \frac{\sin^{-1}(13/24)}{\omega}, \quad t_8 = \frac{\sin^{-1}(15/24)}{\omega}, \quad t_9 = \frac{\sin^{-1}(17/24)}{\omega}, \\ t_{10} &= \frac{\sin^{-1}(19/24)}{\omega}, \quad t_{11} = \frac{\sin^{-1}(21/24)}{\omega}, \quad t_{12} = \frac{\sin^{-1}(23/24)}{\omega}. \end{aligned} \quad (6)$$

The voltage ripple (ΔV_{ripple}) is calculated through Equation (7), and the capacity of the capacitors is calculated by considering the %K voltage drop through Equation (8):

$$\Delta V_{\text{ripple}} = \frac{\Delta Q_C}{C}, \quad (7)$$

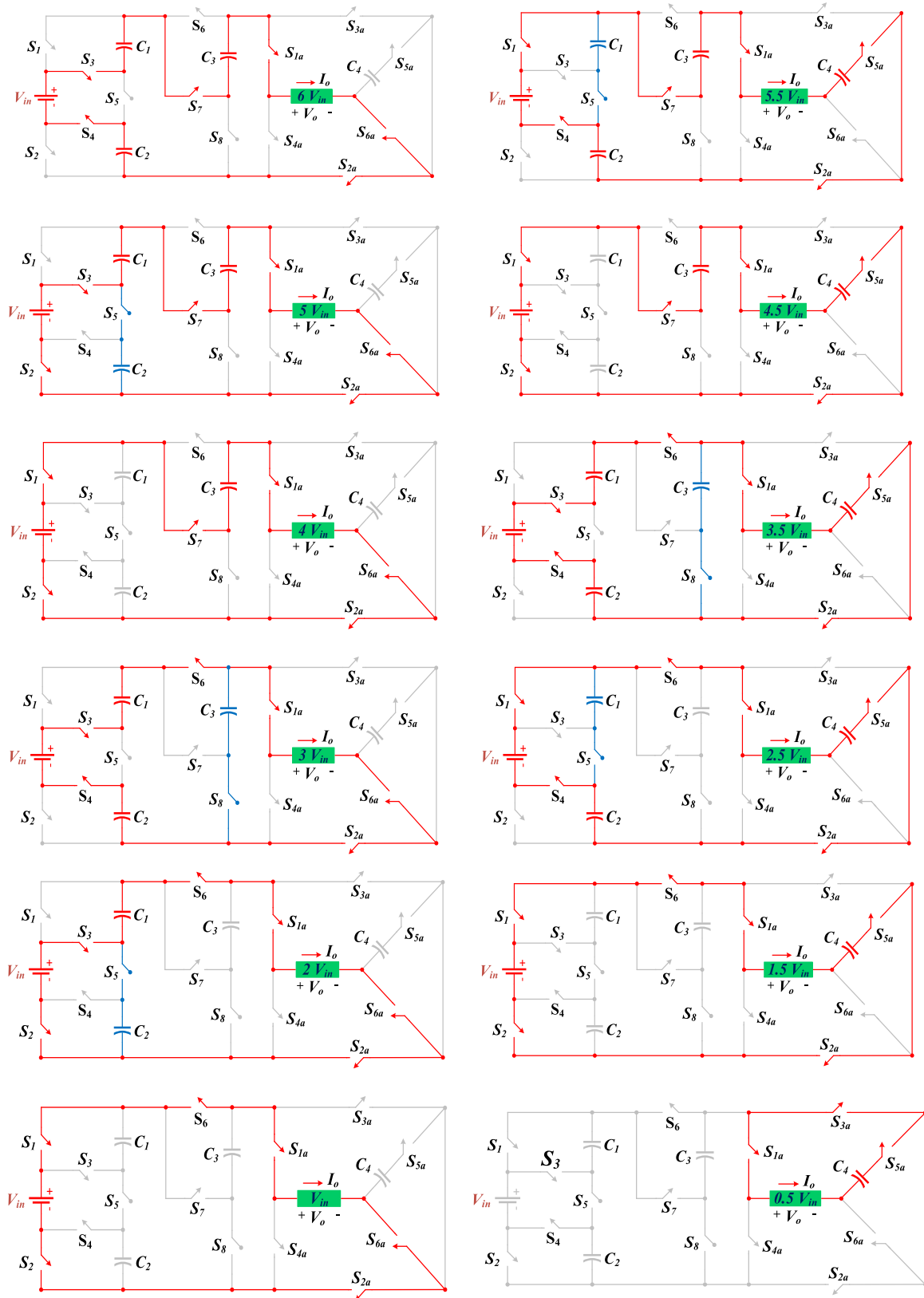


FIGURE 2 The operation states and current paths for the positive half-cycle.

TABLE 2 Current stress of different switches in the proposed topology.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_{1a}	S_{2a}	S_{3a}	S_{4a}	S_{5a}	S_{6a}	V_o
0	0	I_o	I_o	0	0	I_o	0	I_o	I_o	0	0	0	I_o	$6V_{dc}$
$I_o + I_c$	0	0	$I_o + I_c$	$I_o + I_c$	0	I_o	0	I_o	I_o	0	0	I_o	0	$5.5V_{dc}$
0	$I_o + I_c$	$I_o + I_c$	0	$I_o + I_c$	0	I_o	0	I_o	I_o	0	0	0	I_o	$5V_{dc}$
I_o	I_o	0	0	0	0	I_o	0	I_o	I_o	0	0	I_o	0	$4.5V_{dc}$
I_o	I_o	0	0	0	0	I_o	0	I_o	I_o	0	0	0	I_o	$4V_{dc}$
0	0	$I_o + I_c$	$I_o + I_c$	0	$I_o + I_c$	0	$I_o + I_c$	I_o	I_o	0	0	I_o	0	$3.5V_{dc}$
0	0	$I_o + I_c$	$I_o + I_c$	0	$I_o + I_c$	0	$I_o + I_c$	I_o	I_o	0	0	0	I_o	$3V_{dc}$
$I_o + I_c$	0	0	$I_o + I_c$	$I_o + I_c$	I_o	0	0	I_o	I_o	0	0	I_o	0	$2.5V_{dc}$
0	$I_o + I_c$	$I_o + I_c$	0	$I_o + I_c$	I_o	0	0	I_o	I_o	0	0	0	I_o	$2V_{dc}$
I_o	I_o	0	0	0	I_o	0	0	I_o	I_o	0	0	I_o	0	$1.5V_{dc}$
I_o	I_o	0	0	0	I_o	0	0	I_o	I_o	0	0	0	I_o	V_{dc}
0	0	0	0	0	0	0	0	I_o	0	I_o	0	I_o	0	$0.5V_{dc}$
$I_o + I_c$	0	0	$I_o + I_c$	$I_o + I_c$	0	0	0	0	I_o	0	I_o	0	I_o	0
$I_o + I_c$	$I_o + I_c$	0	0	0	$I_o + I_c$	0	0	0	0	$I_o + I_c$	$I_o + I_c$	$I_o + I_c$	0	$-0.5V_{dc}$
I_o	I_o	0	0	0	I_o	0	0	0	0	I_o	I_o	0	I_o	$-V_{dc}$
$I_o + I_c$	0	0	$I_o + I_c$	$I_o + I_c$	$I_o + I_c$	0	0	0	0	$I_o + I_c$	$I_o + I_c$	$I_o + I_c$	0	$-1.5V_{dc}$
0	$I_o + I_c$	$I_o + I_c$	0	$I_o + I_c$	I_o	0	0	0	0	I_o	I_o	0	I_o	$-2V_{dc}$
0	0	$I_o + I_c$	$I_o + I_c$	0	$I_o + I_c$	0	$I_o + I_c$	0	0	$I_o + I_c$	$I_o + I_c$	$I_o + I_c$	0	$-2.5V_{dc}$
0	0	$I_o + I_c$	$I_o + I_c$	0	$I_o + I_c$	0	$I_o + I_c$	0	0	I_o	I_o	0	I_o	$-3V_{dc}$
$I_o + I_c$	$I_o + I_c$	0	0	0	0	$I_o + I_c$	0	0	0	$I_o + I_c$	$I_o + I_c$	$I_o + I_c$	0	$-3.5V_{dc}$
I_o	I_o	0	0	0	0	I_o	0	0	0	I_o	I_o	0	I_o	$-4V_{dc}$
$I_o + I_c$	0	0	$I_o + I_c$	$I_o + I_c$	0	$I_o + I_c$	0	0	0	$I_o + I_c$	$I_o + I_c$	$I_o + I_c$	0	$-4.5V_{dc}$
0	$I_o + I_c$	$I_o + I_c$	0	$I_o + I_c$	0	I_o	0	0	0	I_o	I_o	0	I_o	$-5V_{dc}$
0	0	$I_o + I_c$	$I_o + I_c$	0	0	$I_o + I_c$	0	0	0	$I_o + I_c$	$I_o + I_c$	$I_o + I_c$	0	$-5.5V_{dc}$
0	0	I_o	I_o	0	0	I_o	0	0	0	I_o	I_o	0	I_o	$-6V_{dc}$

$$C_1 \geq \frac{\Delta Q_{C_2}}{K V_{in}}, \quad C_2 \geq \frac{\Delta Q_{C_2}}{K V_{in}}, \quad C_3 \geq \frac{\Delta Q_{C_3}}{K(3V_{in})}, \quad (8)$$

$$C_4 \geq \frac{\Delta Q_{C_4}}{K(0.5V_{in})}.$$

By calculating and placing the above parameters, the final equation of capacitors capacity is expressed according to (9)–(12):

$$C_1 \geq \frac{2I_o}{K\omega V_{in}} [\cos(2\pi f t_{11} - \varphi) - \sin \varphi], \quad (9)$$

$$C_2 \geq \frac{2I_o}{K\omega V_{in}} [\cos(2\pi f t_9 - \varphi) - \sin \varphi], \quad (10)$$

$$C_3 \geq \frac{2I_o}{K\omega 3V_{in}} [\cos(2\pi f t_7 - \varphi) - \sin \varphi], \quad (11)$$

$$C_4 \geq \frac{6I_o}{K\omega 0.5V_{in}} \left\{ \begin{array}{l} [\cos(2\pi f t_1 - \varphi) - \cos(2\pi f t_2 - \varphi)] \\ + [\cos(2\pi f t_3 - \varphi) - \cos(2\pi f t_4 - \varphi)] \\ + [\cos(2\pi f t_5 - \varphi) - \cos(2\pi f t_6 - \varphi)] \\ + [\cos(2\pi f t_7 - \varphi) - \cos(2\pi f t_8 - \varphi)] \\ + [\cos(2\pi f t_9 - \varphi) - \cos(2\pi f t_{10} - \varphi)] \\ + [\cos(2\pi f t_{11} - \varphi) - \cos(2\pi f t_{12} - \varphi)] \end{array} \right\}. \quad (12)$$

The inductor (L_r) in the proposed inverter is used to limit the inrush current of the capacitors and limit the power loss which arises from inrush current of capacitors. The size of this small charging inductor is calculated by taking into account the fact that the charging process of the capacitors should complete

TABLE 3 Voltage stress of different switches in the proposed topology ($\times V_{dc}$).

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_{1a}	S_{2a}	S_{3a}	S_{4a}	S_{5a}	S_{6a}	V_o
1	1	0	0	1	3	0	3	0	0	6	6	0.5	0	$6V_{dc}$
0	1	1	0	0	3	0	2	0	0	5	5	0	0.5	$5.5V_{dc}$
1	0	0	1	0	3	0	2	0	0	5	5	0.5	0	$5V_{dc}$
0	0	1	1	1	3	0	2	0	0	4	4	0	0.5	$4.5V_{dc}$
0	0	1	1	1	3	0	2	0	0	4	4	0.5	0	$4V_{dc}$
1	1	0	0	1	0	3	0	0	0	3	3	0	0.5	$3.5V_{dc}$
1	1	0	0	1	0	3	0	0	0	3	3	0.5	0	$3V_{dc}$
0	1	1	0	0	0	3	0	0	0	2	2	0	0.5	$2.5V_{dc}$
1	0	0	1	0	0	3	0	0	0	2	2	0.5	0	$2V_{dc}$
0	0	1	1	1	3	2	0	0	1	1	0	0	0.5	$1.5V_{dc}$
0	0	1	1	1	3	2	0	0	1	1	0.5	0.5	0	V_{dc}
0.5	0.5	0.5	0.5	0	3	1	0	2	0	2	0	0	0.5	$0.5V_{dc}$
0	1	1	0	0	0	3	1	2	0	2	0	0.5	0	0
0	0	1	1	1	0	3	2	3	1	0	0	0	0.5	$-0.5V_{dc}$
0	0	1	1	1	0	3	2	3	3	0	0	0.5	0	$-V_{dc}$
0	1	1	0	0	0	3	1	2	2	0	0	0	0.5	$-1.5V_{dc}$
1	0	0	1	0	0	3	0	2	2	0	0	0.5	0	$-2V_{dc}$
1	1	0	0	1	0	3	0	3	3	0	0	0	0.5	$-2.5V_{dc}$
1	1	0	0	1	0	3	0	3	3	0	0	0.5	0	$-3V_{dc}$
0	0	1	1	1	3	0	2	4	4	0	0	0	0.5	$-3.5V_{dc}$
0	0	1	1	1	3	0	2	4	4	0	0	0.5	0	$-4V_{dc}$
0	1	1	0	0	3	0	2	5	5	0	0	0	0.5	$-4.5V_{dc}$
1	0	0	1	0	3	0	2	5	5	0	0	0.5	0	$-5V_{dc}$
1	1	0	0	1	3	0	3	6	6	0	0	0	0.5	$-5.5V_{dc}$
1	1	0	0	1	3	0	3	6	6	0	0	0.5	0	$-6V_{dc}$

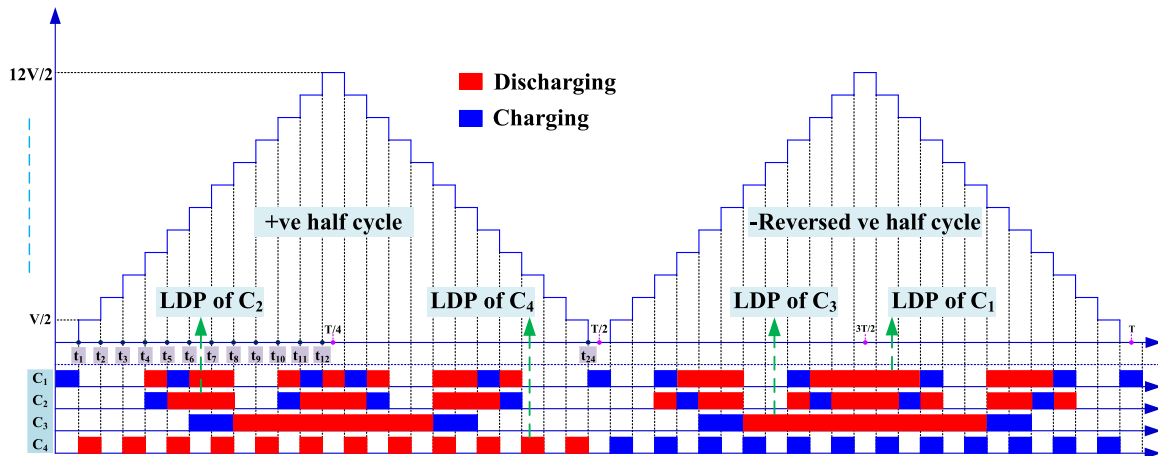


FIGURE 3 The charge and discharge pattern of the capacitors for different voltage levels. LDP, largest discharging period.

during a switching interval.²⁹ In other words, the resonant frequency (f_r) of charging inductor and the capacitor should be lower than the switching frequency (f_s).³⁰ So, the charging inductor (L_r) can be calculated according to Equation (14).

$$f_r = \frac{1}{2\pi\sqrt{L_r C}} < f_{sw} \Rightarrow L_r = \frac{1}{(2\pi f_s)^2 C}. \quad (13)$$

2.2 | Modulation strategy

There are different methods for switching multilevel inverters, which are generally classified into two categories: high-frequency and low-frequency modulation schemes. Sinusoidal Pulse Width Modulation and space vector modulation techniques are high-frequency switching. On the other hand, fundamental frequency switching, nearest level control (NLC), selective harmonic elimination, and active harmonic elimination switching are also low-frequency modulation methods. The NLC switching scheme has been utilized for switching and controlling the switches of the proposed structure. Figure 4 displays the implemented control plan. In this control method, voltage levels are generated by considering the value of the sinusoidal signal as an integer so that it is close to the nearest voltage level. For example, when the instantaneous value of the sinusoidal signal is in the range of 2.5–3.5, the voltage level of $3V_{dc}$ will be generated.

2.3 | Expanded structure

The proposed structure can be extended by incorporating an SC module to produce higher levels. The proposed extended structure is shown in Figure 5. In other words, by adding two switches, a diode, and a capacitor to the proposed structure, the output voltage levels can be increased to 37 levels. In this case, the voltage of the capacitor C_{1c} is stabilized at $3V_{dc}$, and the voltage boost factor is equal to 9. By combining n SC modules in the proposed structure, higher voltage levels can be accessed, in which case the C_n capacitors are jointly charged through the S_8 switch. On the other hand, capacitors will be discharged through $S_{(n+1)c}$ switches. For the generalized structure, the number of switches (N_{sw}), the number of drivers (N_{dr}), the number of voltage sources (N_{dc}), the number of capacitors (N_{cap}), the voltage gain ($Gain$), the number of diodes (N_{dd}), and the number of voltage levels (N_l) can be calculated, respectively, according to the following relations:

$$N_{sw} = 2n + 14, \quad (14)$$

$$N_{dr} = 2n + 14, \quad (15)$$

$$N_{dc} = 1, \quad (16)$$

$$N_{cap} = n + 4, \quad (17)$$

$$Gain = 3n + 6, \quad (18)$$

$$N_{dd} = 1, \quad (19)$$

$$N_l = 12n + 25. \quad (20)$$

3 | POWER LOSSES EVALUATION

In an SC-based converter, three parameters of switching losses (P_{sw}), ripple losses (P_{rip}), and conduction losses (P_{con}) play a key role in total losses (P_{losses}).^{28,31} The general equation of losses is as follows, and each parameter is evaluated separately.

$$P_{losses} = P_{sw} + P_{rip} + P_{con}. \quad (21)$$

3.1 | Switching losses

The delay in the conduction function of the switches in turning on and turning off, which is related to the nonideality of the switches, leads to energy loss (E_{sw}). The wasted energy during the turning on and off time intervals can be calculated through Equation (22). Therefore, the switching loss during the switching process is according to (23).

$$E_{sw} = \frac{1}{2} C_{oss} V_{block}^2, \quad (22)$$

$$P_{sw} = f_s E_{sw} = \frac{1}{2} f_s C_{oss} V_{block}^2. \quad (23)$$

In this equation, f_s is the switching frequency, C_{oss} is the parasitic capacitor parallel to the switch, and V_{block} is the blocking voltage of the switch when it is off or before it is turned on.

3.2 | Ripple losses

The voltage difference between the capacitors and the DC power supply during charging, which is caused by the internal resistance of the capacitors and the power equipment in the current pass of the capacitors charging, causes ripple losses. The voltage difference ΔV_C , which is a parameter affecting the ripple energy loss (E_{rip}), can be

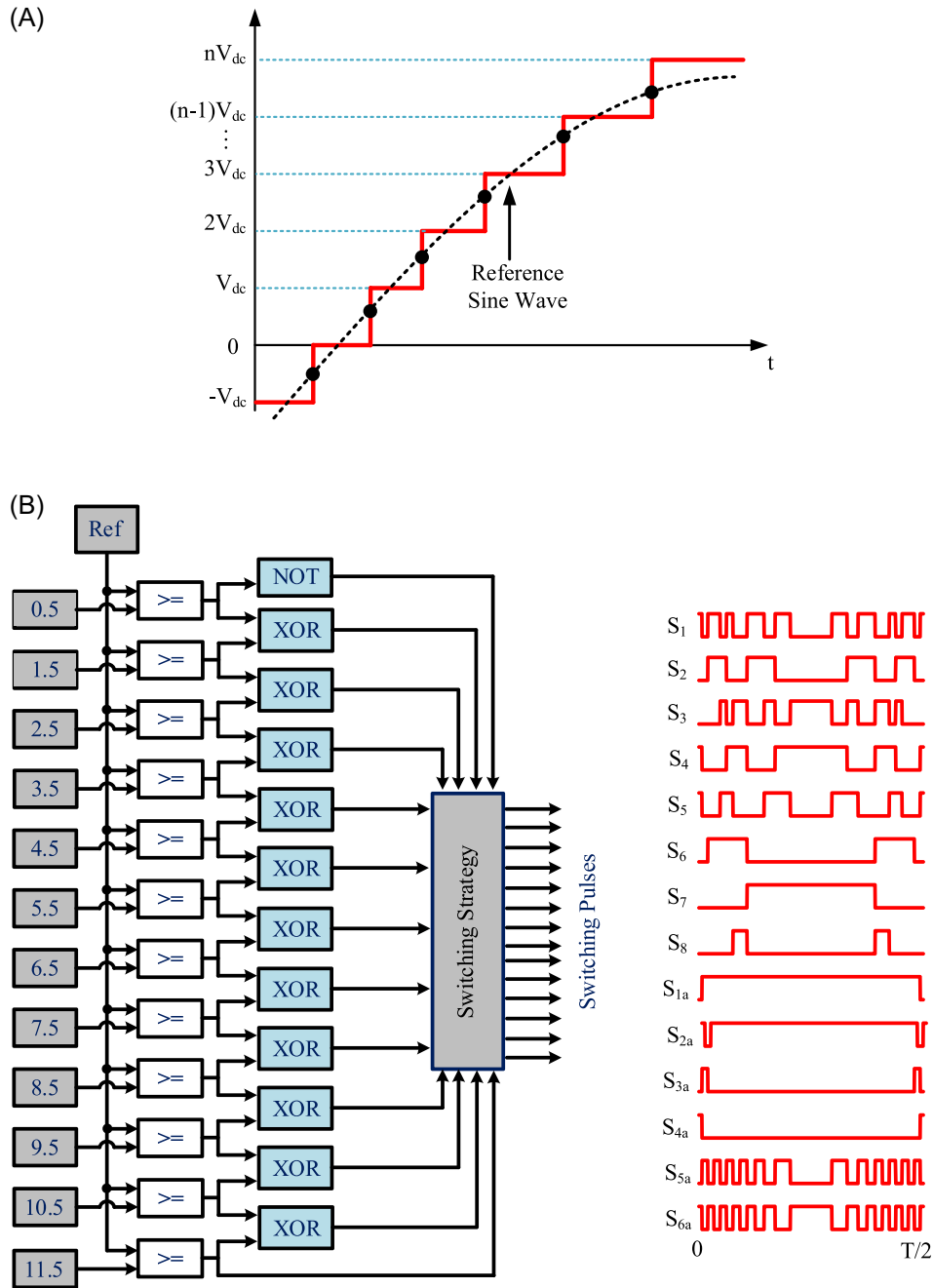


FIGURE 4 Nearest level control (NLC) strategy: (A) NLC technique and (B) half-cycle positive switching logic.

calculated as Equation (24). Besides, the wasted energy (E_{rip}) is calculated from Equation (25).

$$\Delta V_C = \frac{1}{C} \int_0^{t_c} i_C(t) dt, \tag{24}$$

$$E_{rip} = \frac{1}{2} C \Delta V_C^2. \tag{25}$$

Finally, the ripple losses are calculated according to Equations (24) and (25) as follows:

$$P_{rip} = f_0 E_{rip} = \frac{f_0}{2C} \left[\int_0^{t_c} I_C(t) dt \right]^2. \tag{26}$$

3.3 | Conductive losses

Conduction losses of switches in the on state depend on the internal resistance of switches (r_s). Also, the losses on the internal resistance of capacitors (r_c) are the most critical losses for an SC converter. Figure 6 illustrates the equivalent circuit related to the conduction losses of the

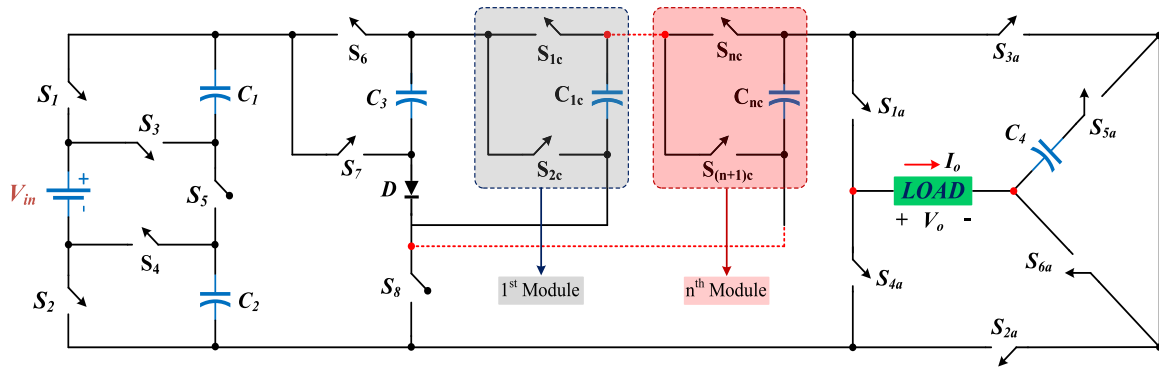


FIGURE 5 The proposed extended structure.

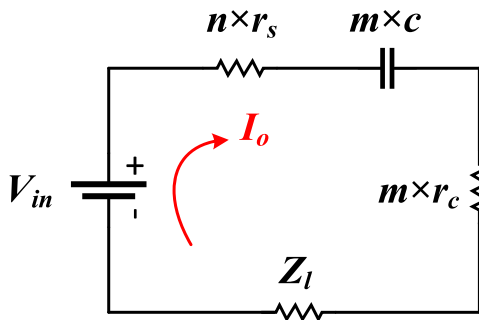


FIGURE 6 Equivalent circuit related to conductive losses of the elements of the proposed structure.

elements of the proposed structure, where $n \times r_s$ is the number of internal resistance of switches, $m \times c$ is the number of capacitors and $m \times r_c$ is the number of internal resistance of capacitors in the current pass of each operation state. Further, I_o is the output current and is obtained from Equation (27). In this equation, M_a is the modulation index, and Z_l is the load impedance.

$$I_o = I_o \sin \omega t = \frac{M_a \times 6V_{in}}{Z_l} \sin \omega t. \quad (27)$$

Considering the time interval corresponding to each voltage level, it is possible to evaluate the conduction losses. For example, in Figure 3, the (t_1-t_2) time interval corresponds to the generation of the $0.5V_{dc}$ level. Hence, conduction losses are expressed according to Equation (28):

$$E_{con}(0.5V_{in}) = \int_{t_1}^{t_2} I_o^2(3r_s + r_c) dt. \quad (28)$$

In this way, conduction losses are calculated for all states of voltage levels according to Equation (29), and their sum is considered total conduction losses. As a result, by calculating the parameters related to the

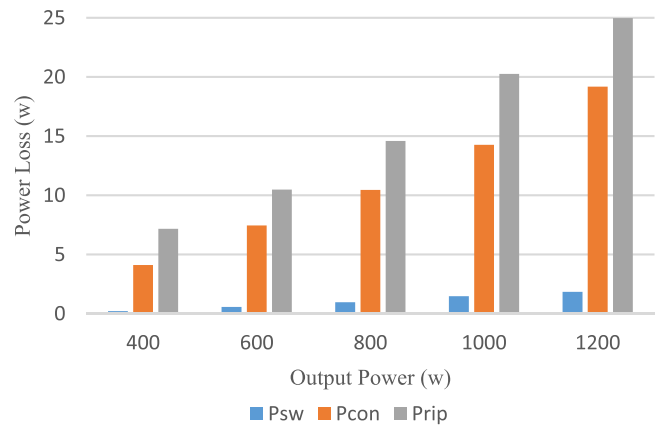


FIGURE 7 Diagram of converter losses for different powers.

converter losses, the converter's efficiency can be calculated through Equation (30). In this equation, P_{out} is the output power of the converter. Figure 7 displays the converter losses for different output power.

$$P_{con} = 12f_0 \sum_{i=0.5,1, \dots, 6} E_{con(i)}, \quad (29)$$

$$\eta = \frac{P_{out}}{P_{out} + P_{sw} + P_{rip} + P_{con}}. \quad (30)$$

4 | COMPARATIVE EVALUATION

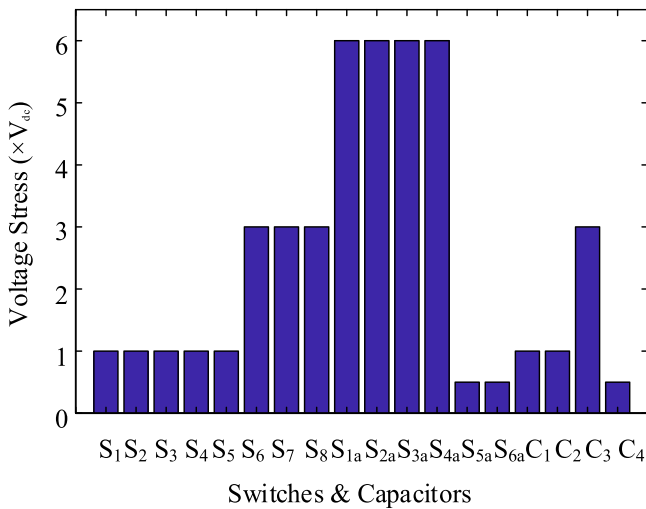
In this section, to examine the advantages and disadvantages of the proposed structure, a comparison has been made with other SC structures in Table 4. Comparative parameters including the number of input sources (N_{dc}), the number of switches (N_{sw}), the number of drivers (N_{dr}), the number of output voltage levels (N_l), the number of diodes (N_{dd}), the number of capacitors (N_{cap}), the maximum standing voltage of all switches

TABLE 4 Comparison of the proposed structure with other 25-level structures.

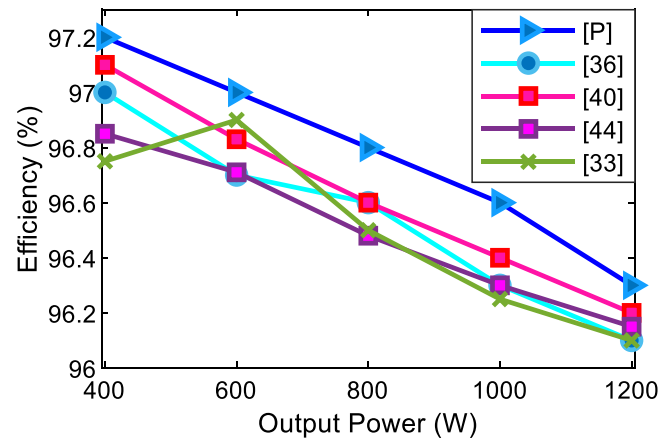
Topology	N_{dc}	N_l	N_{sw}	N_{dr}	N_{dd}	N_{cap}	$TSV (\times V_{in})$	Gain	C_f
[35]	1	25	35	34	2	7	49	6	5.08
[33]	2	25	13	12	0	2	39	2	5.28
[32]	1	25	21	21	2	5	51	12	4
[36]	1	25	15	15	2	4	39	6	3
[34]	2	25	12	12	2	2	21	2	3.92
[18]	1	25	19	19	2	4	58	12	4.08
[37]	2	25	14	12	2	2	52	2	6.56
[38]	2	25	18	14	2	4	40	4	6.24
[19]	2	25	11	11	12	6	28	1	5.44
[39]	6	25	30	30	6	6	60	12	31.68
[20]	1	25	16	16	3	4	56	12	3.8
[40]	1	25	16	16	6	6	54	6	3.92
[41]	1	25	16	14	6	6	47	12	3.56
Proposed	1	25	14	14	2	4	39	6	2.92

Note: N_{dc} is number dc sources, N_l is number output voltage levels, N_{sw} is number of switches, N_{dr} is number of gate drivers, N_{dd} is number of diodes, N_{cap} is number of capacitors, and C_f represents the cost factor.

Abbreviation: TSV, total standing voltage.


FIGURE 8 Voltage stress of the switches and the capacitors.

(TSV), and the gain are reviewed for recently introduced converters. Although the structures in Singh and Mandal¹⁸ and Sandeep³² have a higher boost factor, their component count is too high compared to generated levels. In addition, the structures presented in Bana et al.³³ and Murshid et al.³⁴ have a relatively minor number of switches, drivers, and capacitors. Still, these structures are not single sources and are investigated in an asymmetric configuration. To estimate the total cost of the converter, the cost factor of the converter is


FIGURE 9 Efficiency comparing the proposed structure with other structures in different output power.

introduced in Equation (31). According to Table 4, the proposed converter has significant superiority in cost factor versus the compared structures. Figure 8 presents the value of the blocked voltage on each switch. Also, the comparison of the efficiency of the proposed structure with other structures for different output powers is shown in Figure 9. The cost of semiconductor equipment and gate driver of the proposed structure and other single-source structures are presented in Table 5. It should be noted that this table only includes the cost of power electronic equipment for comparison. Naturally,

TABLE 5 Cost comparison of the proposed structure and other structure.

Components	Part number	Voltage rating	Unit price (\$)	[35]	[36]	[18]	[20]	[40]	[41]	P
MOSFET	FDP51N25	250 V	2.92	×14	×7	×8	×8	×4	×4	×7
	FDA24N40F	400 V	3.62	×21	×4	×11	×8	×8	×12	×3
	SIHP080N60E-GE3	600 V	4.41	–	×4	–	–	×4	–	×4
Capacitor	PEH534PDF4390M2	100 V 3900 μF	11.69	–	×1	×1	×1	×2	×3	×1
	LKG1H472MESCK	50 V 4700 μF	10.51	–	×1	–	–	–	–	×1
	ALC80A472DF100	100 V 4700 μF	12.57	×2	×1	×1	–	×4	–	×1
	ALF40C392EP200	200 V 3900 μF	15.55	×3	–	×2	×3	–	×3	–
Diode	P600D-E3/54	200 V	0.94	×2	×2	×2	×1	×2	–	×1
	P600G-E3/54	400 V	0.92	–	–	–	×2	×4	×6	–
Gate driver	IR2102STRPBF	600 V	3.53	×35	×11	×19	×16	×12	×14	×10
	IR2213PBF (dual)	1200 V	7.63	–	×2	–	–	×2	–	×2
Total cost (\$) ^a				314	143	187	169	195	191	135

^aPrices are subject to change.

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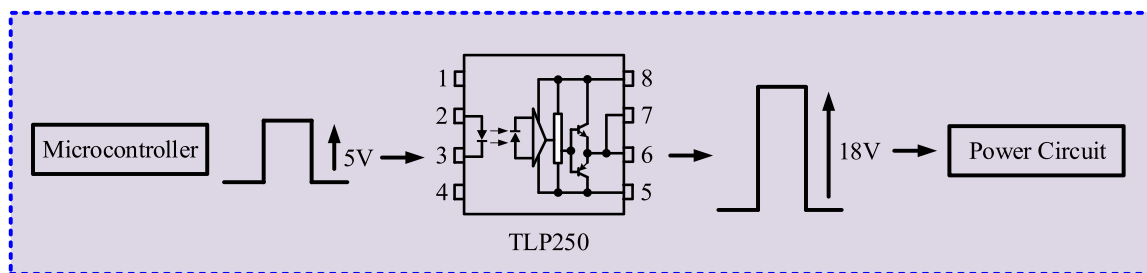


FIGURE 10 Schematic representation of gate driver circuit of switches.

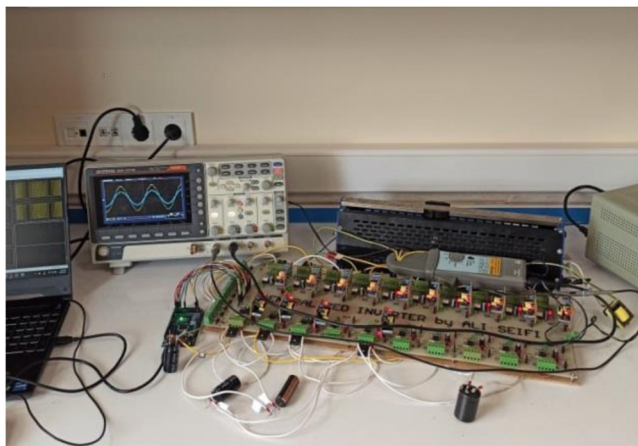


FIGURE 11 The experimental sample of the proposed inverter.

considering the cost of the DC voltage source and the equipment for switch driver circuits, the superiority of the proposed structure's cost will be more pronounced.

$$C_f = \frac{(N_{sw} + N_{dr} + N_{dd} + N_{cap} + TSV)N_{dc}}{N_f}. \quad (31)$$

5 | SIMULATION AND LABORATORY RESULTS

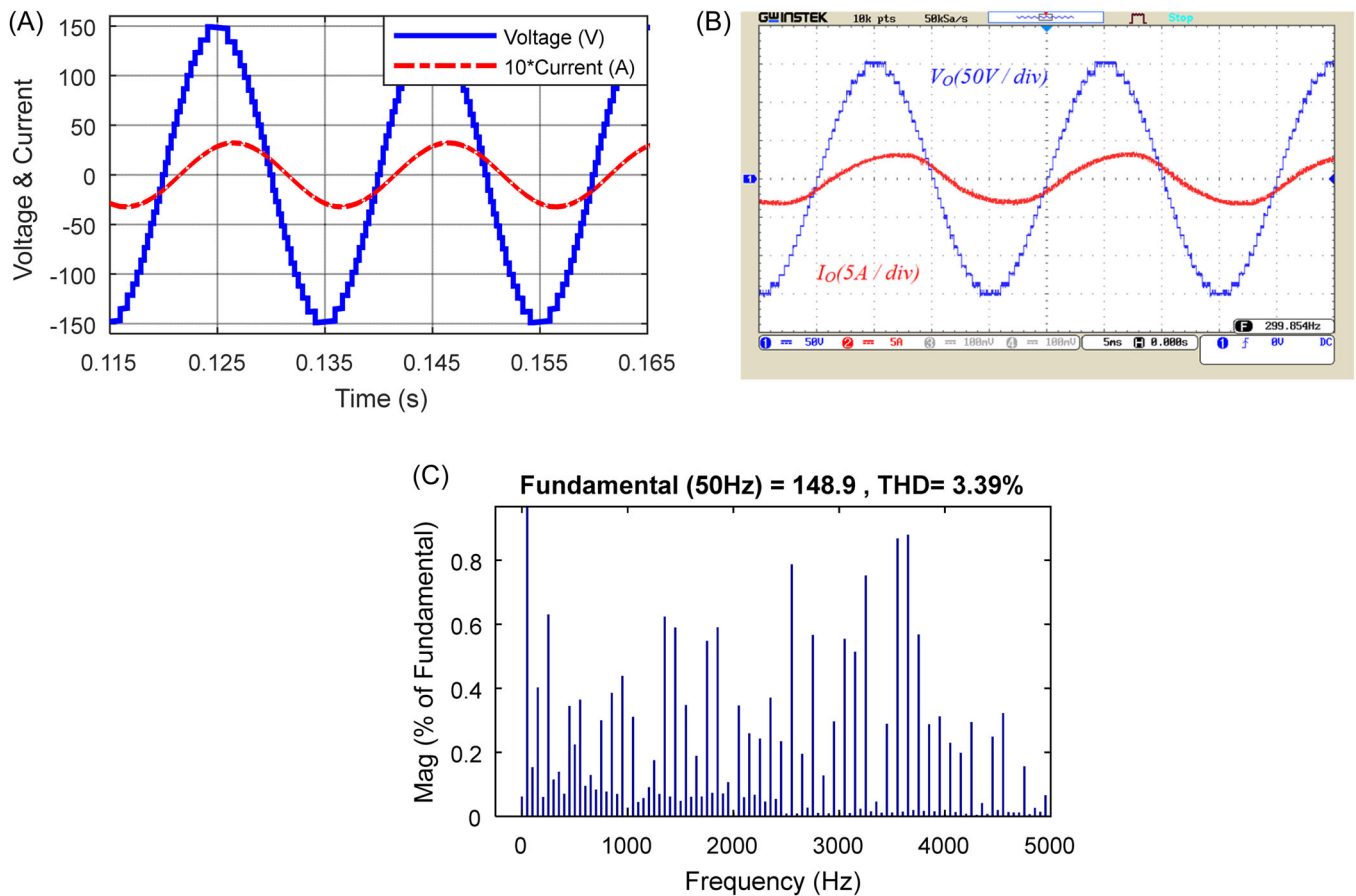
The proposed structure is simulated using the NLC method in MATLAB/Simulink environment. To confirm the correctness of the proposed structure's performance and the results of the simulation, a laboratory prototype

TABLE 6 Simulation and laboratory parameters information.

Parameters	Value
Input voltage	25 V
Output voltage	150 V
Output current	3.3 A
Output frequency	50 Hz
C_1	3700 μF
C_2	4200 μF
C_3	3700 μF
C_4	4200 μF
Load resistance	45 Ω
Load inductance	80 mH
L_r	0.1 mH
MOSFETs	IRFP450
Gate driver	TLP250
Controller	Arduino Mega 2560

is also implemented. The simulation and laboratory results are presented together. Figure 10 depicts the schematic representation of the gate driver circuit of switches in the laboratory sample. Each switch requires an isolated driver circuit. The isolation can be provided using either pulse transformers or optoisolators. Optoisolators can work in a wide range of input signal pulse width, but a separate isolated power supply is required for each switching device. The opto-isolator-based gate driver circuit is used in the implemented laboratory setup. Since the required pulse signal of the MOSFETs is in the range of 15 V, and the peak of the pulse signal generated by the Arduino microcontroller is within the range of 5 V, the pulse signal produced by the microcontroller is amplified and isolated through the TLP250 optocoupler. Figure 11 is related to the laboratory sample. Further, information about simulation and laboratory parameters is shown in Table 6.

Figure 12 displays the output voltage and current waveforms under the R - L load. In Figure 12A, the simulation results are presented. According to this figure,


FIGURE 12 Voltage waveform and output current under resistive-inductive load: (A) simulation results, (B) laboratory results, and (C) output voltage total harmonic distortion. THD, total harmonic distortion.

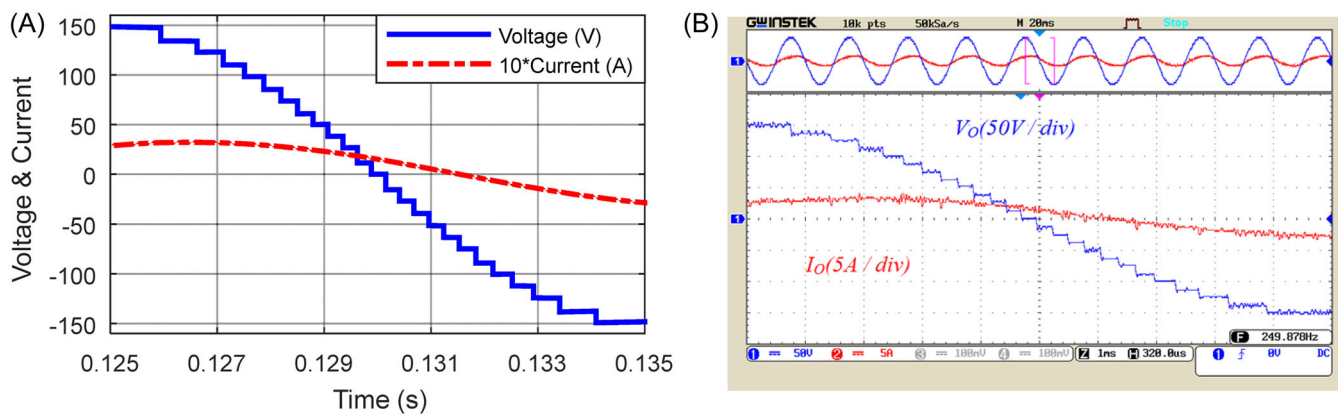


FIGURE 13 Voltage and output current waveforms of the inductive-resistive load and a close-up. (A) Simulation results, (B) Laboratory results.

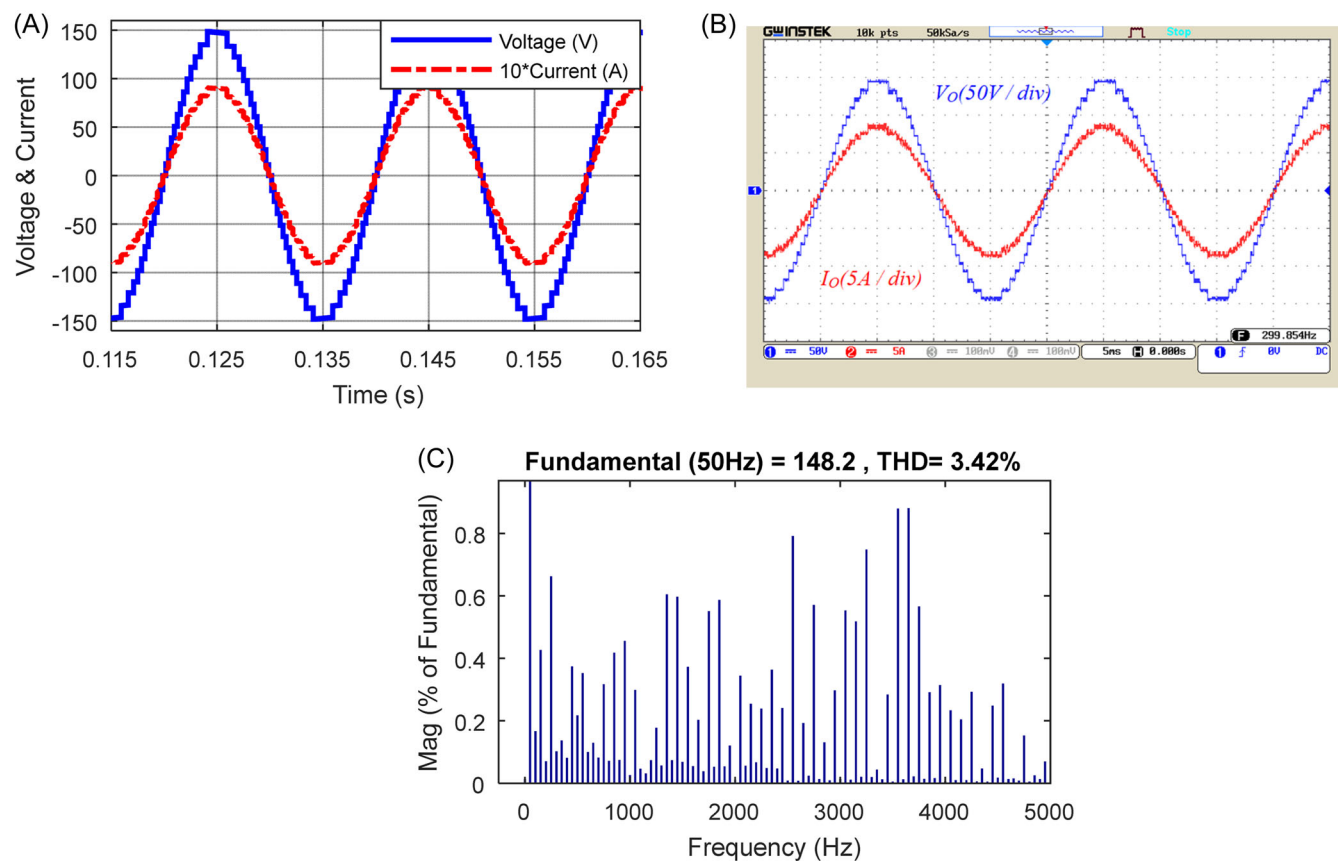


FIGURE 14 Voltage and output current waveform under purely resistive load: (A) simulation results, (B) laboratory results, and (C) output voltage total harmonic distortion. THD, total harmonic distortion.

the output voltage has 25 levels, and each voltage step equals 12.5 V. In Figure 12B, the laboratory results are presented for output voltage and current. Figure 12C illustrates the total harmonic content of the output voltage waveform, where the total harmonic distortion value for 25 voltage is 3.39%. The correspondence

between simulation and laboratory results can be seen in Figure 12.

Figure 13A is related to the simulation results. Figure 13B also relates to the laboratory results for voltage and output current under inductive-resistive load and from a close-up view. The simulation results

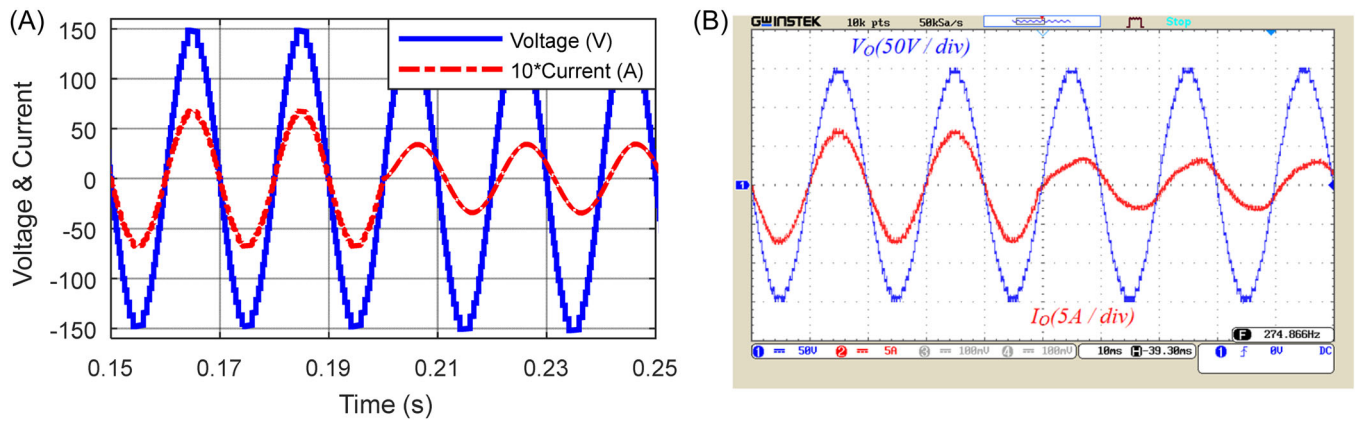


FIGURE 15 Voltage and output current waveform under dynamic load change conditions: (A) simulation results and (B) laboratory results.

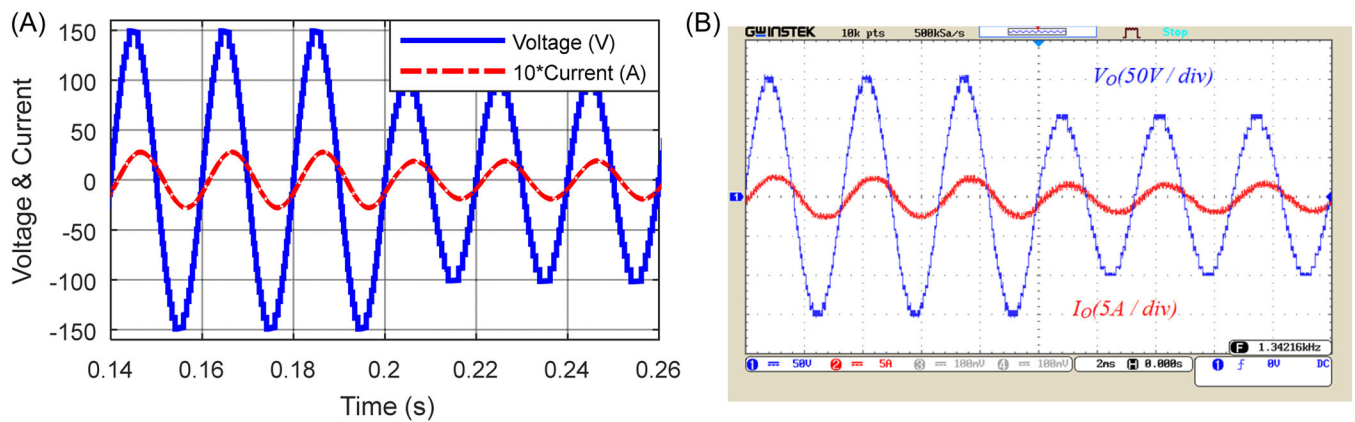


FIGURE 16 Voltage waveform and output current under modulation index dynamic change conditions: (A) simulation results and (B) laboratory results.

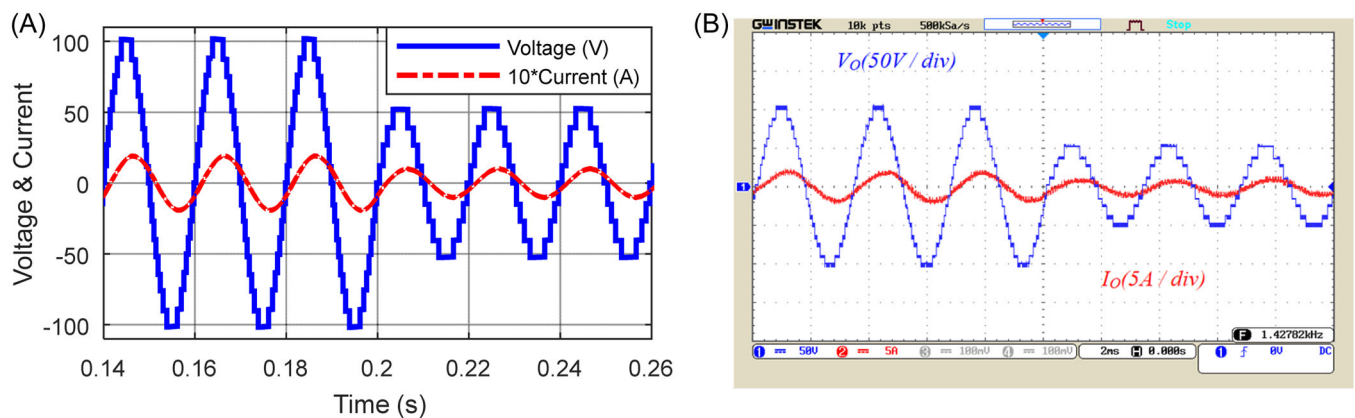


FIGURE 17 Voltage and output current waveform under modulation index dynamic change conditions: (A) simulation results and (B) laboratory results.

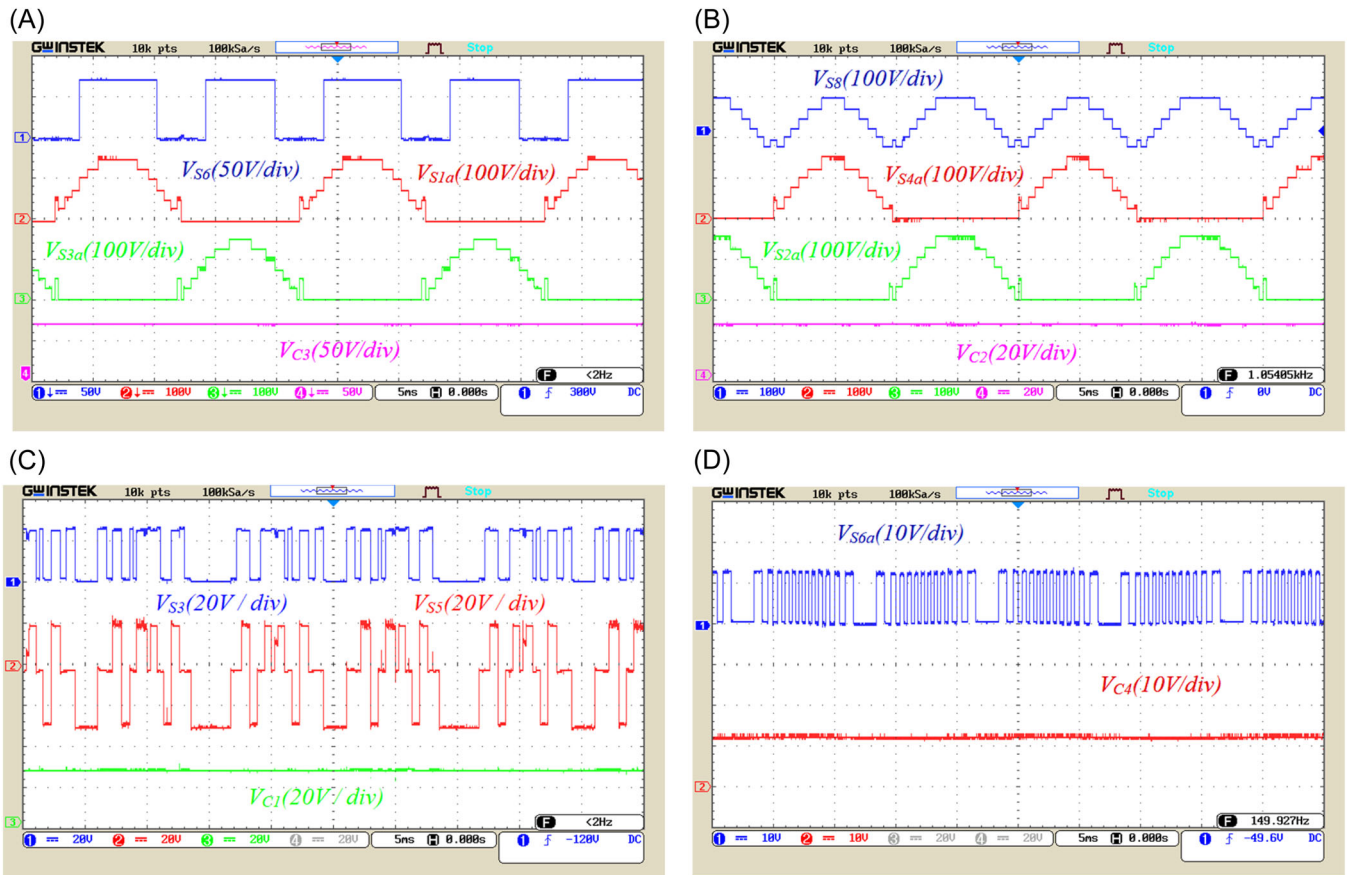


FIGURE 18 (A) Voltage waveform of the S_6 , S_{1a} , and S_{3a} switches and the C_3 capacitor, (B) the voltage waveform of the S_8 , S_{4a} , and S_{2a} switches and the C_2 capacitor, (C) the voltage waveform of the S_3 and S_5 switches and the C_1 capacitor, and (D) the voltage waveform of the S_{6a} switch and the C_4 capacitor.

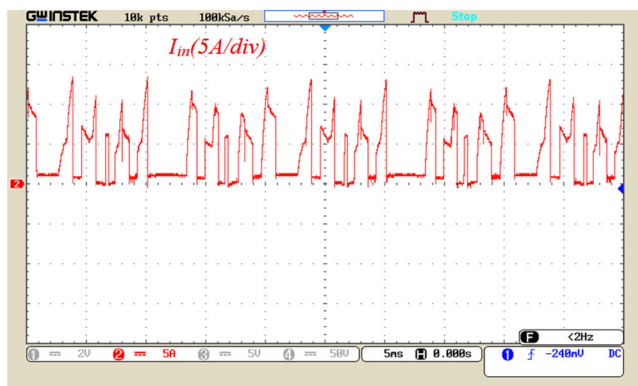


FIGURE 19 Input current waveform.

are presented in Figure 14A, and the laboratory results for output voltage and current under purely resistive load are presented in Figure 14B. In this case, the load resistance is $45\ \Omega$. To show the ability of the proposed inverter in dynamic conditions, the

dynamic load change has been applied. At $t = 0.2\ \text{s}$, the load changes from a purely resistive mode with impedance $Z = 45\ \Omega$ to an inductive-resistive mode with impedance $Z = 45\ \Omega + 80\ \text{mH}$. Figure 15 displays the simulation and laboratory results for output voltage and current under dynamic load change conditions.

Figure 16 shows the changes in voltage and output current waveform during the dynamic change of the modulation index (M_a). On the basis of this figure, at $t = 0.2\ \text{s}$, the modulation index has changed from 1 to 0.65, and as a result, the output voltage levels have decreased from 25 to 17 levels. At the same time, the voltage peak and output current decrease from 150 to 100 V and 3.3 to 1.65 A, respectively.

If the modulation index changes from 0.65 to 0.3 at $t = 0.2\ \text{s}$, according to Figure 17, the output voltage levels vary from 17 to 9. The peak voltage and output current also decrease from 100 to 50 V and 1.65 to 0.825 A, respectively. In this figure, the appropriate performance

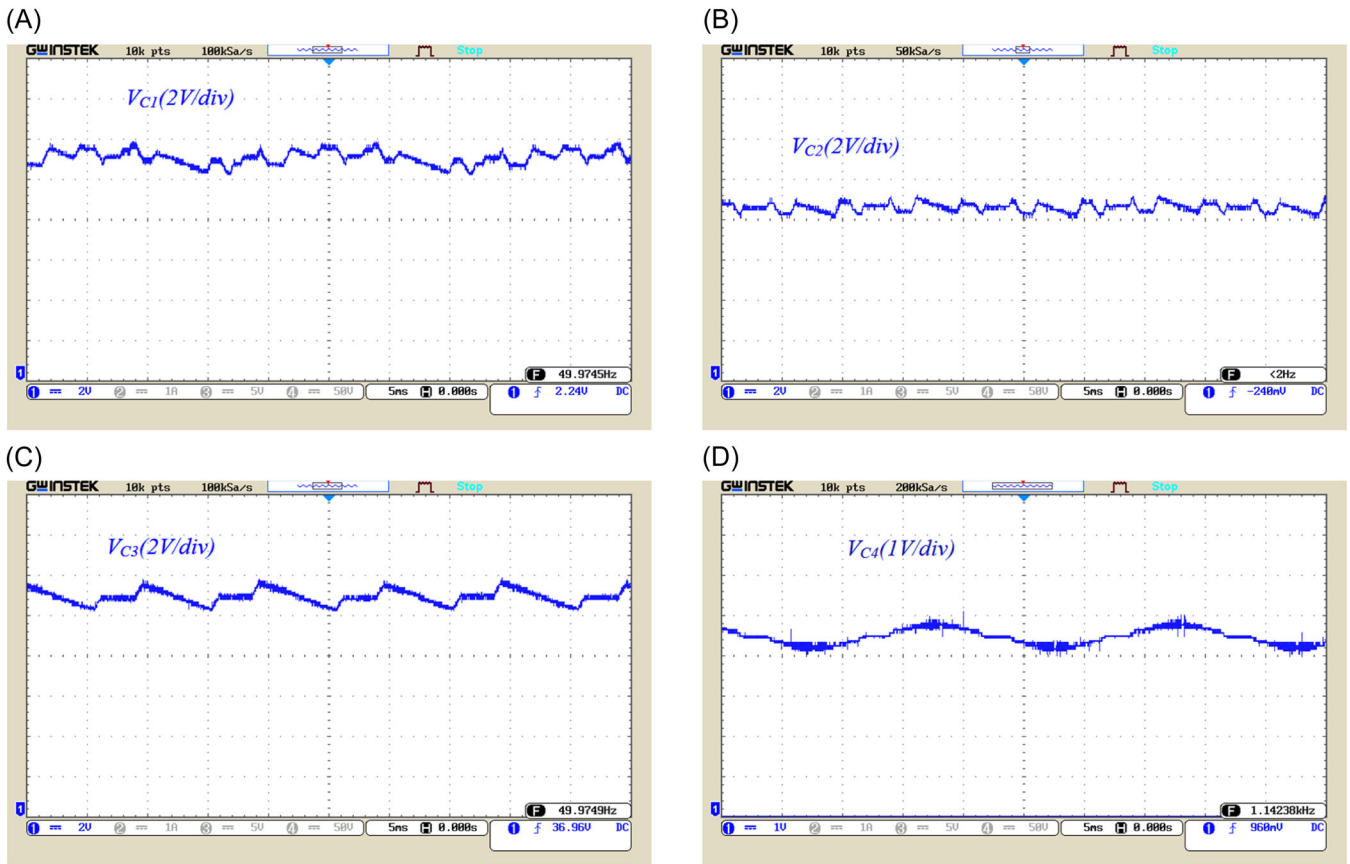


FIGURE 20 Capacitors' voltage waveforms: (A) the voltage ripple of capacitor C_1 , (B) the voltage ripple of capacitor C_2 , (C) the voltage ripple of capacitor C_3 , and (D) the voltage ripple of capacitor C_4 .

of the proposed structure is evident during the dynamic change of the modulation index.

Figure 18A demonstrates the voltage waveform of the switches S_6 , S_{1a} , and S_{3a} and the voltage waveform of the C_3 capacitor. According to this figure, the peak voltage of switch S_6 is 75 V, and the peak voltage of switches S_{1a} and S_{3a} is 150 V. Besides, the voltage of the capacitor C_3 is 75 V. Figure 18B shows the voltage waveform of switches S_8 , S_{4a} , and S_{2a} , along with the voltage waveform of the capacitor C_2 . The peak voltage of the switches S_{4a} and S_{2a} is 150 V, and the peak voltage of the switch S_8 is 75 V. Further, the capacitor C_2 voltage is 25 V. Figure 18C is related to switches S_3 and S_5 voltage and the capacitor C_1 voltage. The peak voltage of each switch is 25 V, and the voltage of the capacitor is also equal to 25 V. Figure 18D shows the voltage waveform of the capacitor S_{6a} switch and C_4 . The peak voltage of the switch S_{6a} as well as the voltage of capacitor C_4 are 12.5 V. According to Figure 18, the correct and suitable operation of the converter and its switches

can be observed. Figure 19 shows the input current waveform. As can be seen in this figure, the input current peak is around 13 A. The voltage waveforms of the capacitors are depicted in Figure 20. As can be observed from this figure, the ripple voltage of the capacitors is within the permissible range. In Figure 21, the waveform of the current for capacitors is presented. The charging current of capacitors C_1 – C_3 is limited by the use of an inductor, leading to an increase in the lifespan of semiconductor equipment. Capacitor C_4 has a lower charging current due to being connected in series with the output load. Additionally, in Figure 22, the current through some switches has been displayed.

The analysis of the converter losses and its efficiency using the nearest level modulation scheme in both the simulation environment and the laboratory environment is investigated in the following. The parasitic parameters of the switches to evaluate the switches losses have been used from the IRFP450 MOSFET datasheet. In the simulation environment, if

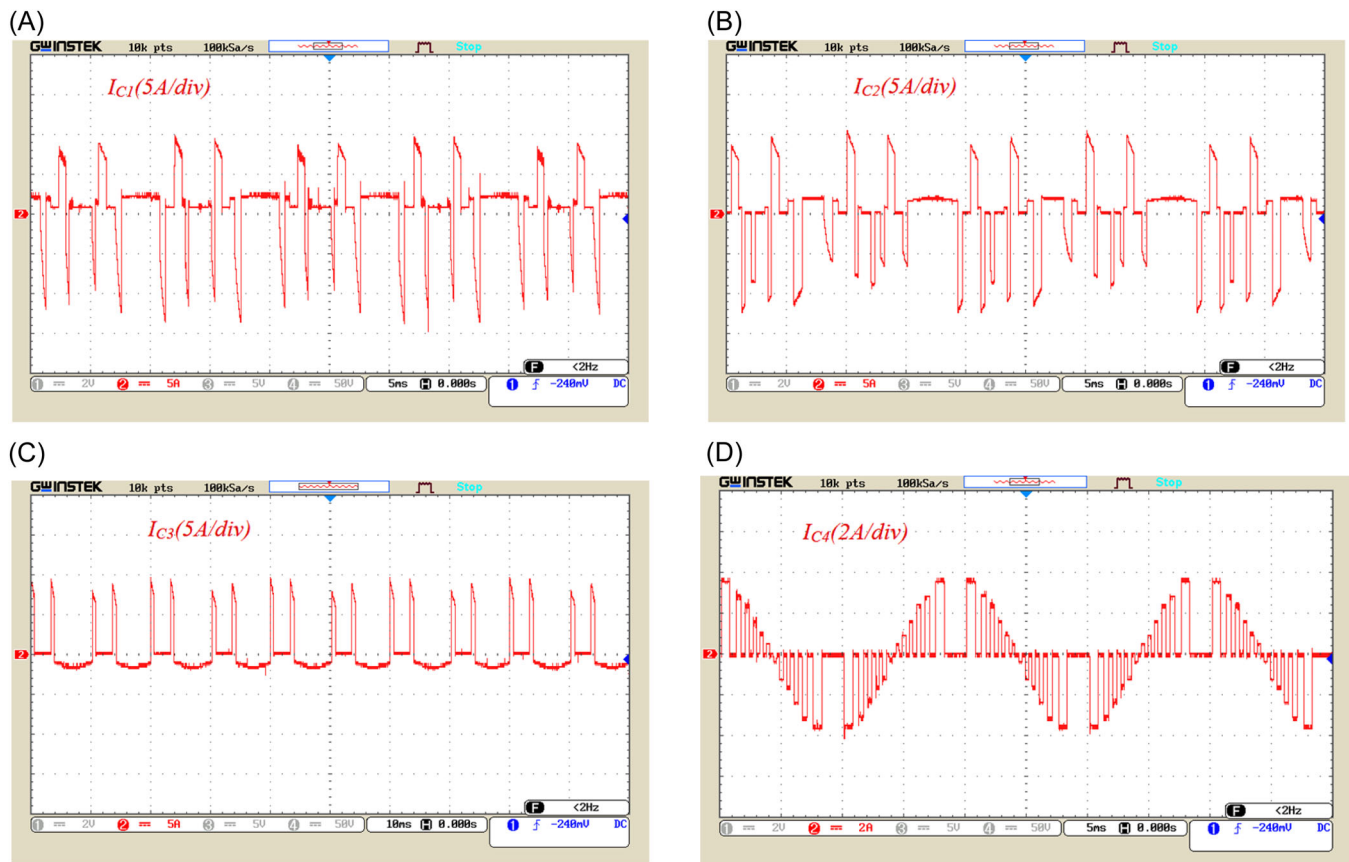


FIGURE 21 Capacitors' current waveforms: (A) the current of capacitor C_1 , (B) the current of capacitor C_2 , (C) the current of capacitor C_3 , and (D) the current of capacitor C_4 .

the input voltage value is equal to 25 V and the output load is an inductive–resistive impedance ($Z_{\text{load}} = 60 \Omega + 80 \text{ mH}$), then the switching losses, conduction losses, ripple losses and output power will be 0.75, 7.45, 10.47, and 600 W, respectively, resulting in 97% efficiency. In the implementation environment and based on the same conditions, the input power is 618.67 W and the output power is 581.54 W. Hence, the converter's loss is 21.16 W and its efficiency is 96.58%. With a pure ohmic load of 60Ω , the simulation shows that switching losses, conduction losses, ripple losses, and output power are 1.4, 12.578, 19.622, and 962.4 W, respectively. The efficiency is also 96.62%. In the implementation environment and with the same conditions, the input power equals 990.92 W, the output power is 952.46 W, the loss is 38.46 W, and the efficiency is 96.11%. Comparing the simulation losses analysis with the efficiency results in the experiment environment depicts a suitable agreement in simulation and implementation results.

6 | CONCLUSION

In this paper, a single-source structure is presented for an SC multilevel inverter with voltage boost capability, and its extended structure is also investigated. The proposed structure can boost the input voltage by six times. A comprehensive comparison has been made between the proposed converter and other recently presented structures regarding the number of elements, TSV, and gain factor. The comparison reveals that the cost factor of the proposed structure is lower than other structures. The operation principles, charging and discharging modes, and current flow paths are presented in detail. The utilized capacitors have been studied, and necessary relationships have been extracted. The proposed structure has advantages, such as a single source, voltage boost capability, self-balancing of capacitors, low voltage stress on most switches, and lower overall cost. The simulation results show the correct performance of the proposed structure, followed by the laboratory results showing a close match with the simulation results.

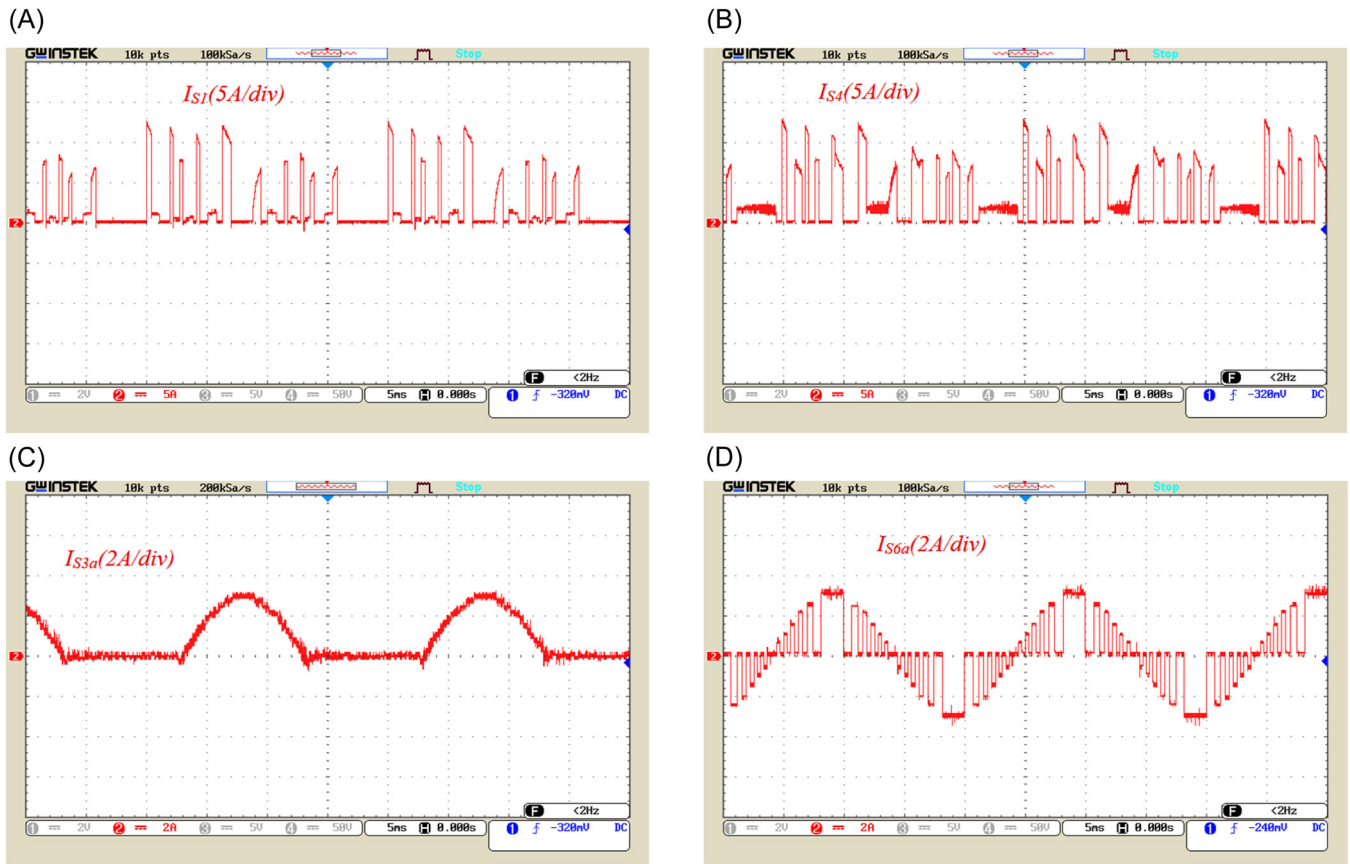


FIGURE 22 The current waveforms of the switches: (A) the current of switch S_1 , (B) the current of switch S_4 , (C) the current of switch S_{3a} , and (D) the current of switch S_{6a} .

NOMENCLATURE

C_f	cost factor
C_{oss}	output capacitance of switch
D_r	parallel diode
f	fundamental frequency ($\omega = 2\pi f$)
f_s	switching frequency
I_c	charging current
I_o	output current
LDP	largest discharging period
L_r	charging inductor
MLI	multilevel inverter
N_l	number of output voltage levels
P_{con}	conduction losses
P_{losses}	total losses
P_{out}	output power
P_{rip}	ripple losses
P_{sw}	switching losses
SC	switched-capacitor
t_1-t_{24}	time for each pulse of the steps (s)
t_c	charging time duration
THD	total harmonic distortion
TSV	total standing voltage
V_{block}	blocking voltage of switch

V_{dc}	input DC voltage
V_o	output voltage
Z_l	load impedance

GREEK SYMBOL

η	efficiency
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