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# Fault Current Limiting Investigation for a Single-Phase Dynamic Voltage Conditioner

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***Abstract*—Fault Current Limiting (FCL), applied in fault current condition, is a strategy to reduce network voltage disturbances. The objective of this research is to investigate different FCL approaches for Dynamic Voltage Conditioner (DVC) system within an example LV radial network, the proposed approach could also be adopted for other electronic devices, as Dynamic Voltage Restorer (DVR). Here, a single-phase DVC has been considered because it is an interesting PQ conditioner for Distribution System Operator (DSO). In this paper, a comparison of performances between different approaches will be considered taking into account: the stress on DVC equipment, that needs to be analyzed in order to protect power electronic components and DC link capacitor bank. Also, in order to guarantee proper and in time opening of upstream circuit breaker, the fault current is analyzed that can be limited but only to a certain amount.**

***Index Terms*--Power quality, Voltage sag, Dynamic Voltage Restorer, Dynamic Voltage Conditioner, Fault Current Limiting.**

## I. INTRODUCTION

Voltage variations is an important issue in modern and smart grid systems [1], [2]. Several solutions have been introduced to deal with such phenomena, especially Dynamic Voltage Restorer (DVR) has been practiced effectively to deal with short-term events [3].

Recently, a device that can perfectly satisfy modern power system requirement has been introduced to the society by authors, named Dynamic Voltage Conditioner (DVC) [4], [5]. DVC systems mostly have been installed and used at MV or LV level in order to compensate voltage variations. Usually it is used to regulate the voltage output by injecting a required voltage and several control methods have been proposed and tested [6]. Considering the fact that DVC is a series connected device, all the load current flows through it and without any FCL function, it should be designed to tolerate full network voltage and large fault current (even if it is for very short time). It should be noted that, in case of any fault, the fault current will flow through the injection transformer and into the DVC converter before the circuit breaker open, and without proper considerations this could damage the system.

Therefore, it is important to solve two main problems: the first one related to the DVC components damaging, and the second one related to find a strategy to reduce the network voltage variation.

To solve the first one it is enough to switch-off or by-pass the device, instead to solve the second it should be necessary to reduce the short circuit current peak and average value by integrating proper FCL strategy [7], [8] in the DVC.

Generally, two main FCL methods have been proposed for DVC systems. The first method is to use passive elements in order to limit fault current. As it is proposed in [9], the idea behind this type of control is to use DVC transformer and DVC converter output LC filter to limit the fault current bypassing the converter to avoid any damage to DC link capacitor and switching parts. The second method is to implement active FCL control methods which are integrated into the DVC system controller in order to use DVC converter during fault conditions to limit the fault current [10], [11]. The idea is to inject proper voltage during fault condition that enables the DVC systems to work as impedance to limit the fault current.

This paper investigates different FCL approaches for the DVC system within an example LV radial network, even if, the proposed approach could be adopted for DVR because the fault condition is a short-event. The comparison between the performance of different approaches will be considered from different point of views. First of all, the stress on DVC equipment, such as power electronic components and DC link capacitor bank is considered. From network security point of view, the fault current can be limited in order to reduce the voltage variation at the main bus. However, limiting the fault current, opening time and thresholds of upstream circuit breaker need to be taken into account.

## II. FAULT ANALYSIS

Standards ER G7/4 and IEC 60909 give calculation strategies for short circuits current. In IEC 60947-2, IEC 60898-1 and ANSI C37.13 the standard definitions and terminology for short circuit, circuit breakers and fuses are considered for this work. Usually the short circuit current calculations are made at the system design stage to determine the short circuit ratings of installed devices. Routine calculations are also made to check the continued adequacy of existing equipment as system operating configurations are modified in different ways. Therefore, the maximum short circuit current calculations are carried out for sizing and designing the substations, grid and utilities.

Calculation of minimum short circuit currents are also carried out and used in the adjustment of protection relay settings to ensure accurate and coordinated relay operations.

So, it is very important to evaluate both currents any time a new auxiliary electrical power system, including custom power system devices, are inserted into a network.

Therefore, taking into account a radial LV network described in Fig. 1 it is possible to evaluate this current. The short circuit current consists of AC and transient DC components. The initial magnitude of the DC current component depends on the instant of the voltage waveform when the short circuit occurs. The rate of decay of the DC current component depends on the circuit time constant *L/R*. The assumption of a constant *L* results in a time-independent *L/R* ratio or constant rate of decay.

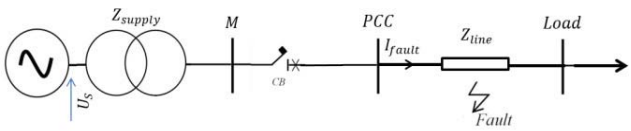


Figure 1 Test network in fault condition

If the supply voltage is equal to $u_s(t) = \sqrt{2} \cdot U_s \cdot \sin(\omega t)$, the short circuit current due to fault at any point downstream the M-bus can be calculated using the Equation (1).

$$i_{fault}(t) = \frac{\sqrt{2} \cdot U_s}{|\underline{Z}_f|} \cdot \sin(\omega t - \angle \underline{Z}_f) + I'' \cdot e^{-\frac{\omega(t - t_{fault})}{\tau}} \qquad (1)$$

Where $\underline{Z}_f$ is the total impedance between the supply and the fault location, $t_{fault}$ is the fault moment and $\tau$ is the time constant in the faulted network which defines the rate of decay of DC current component. The value of integration constant *I*" depends on the fault location and the fault moment. The simulation results in Matlab environment for the maximum and minimum short circuit current in the network, with the parameters given in Table I, are illustrated in Fig. 2.

TABLE I. UNDER STUDY NETWORK PARAMETERS

| ***Parameters*** | ***Values*** |
|---|---|
| Distribution supply voltage | 20kV |
| Distribution transformer ratio | 20kV/230V |
| $Z_{sc}$ Distribution transformer | 4% |
| Injection transformer ratio | 230V/230V |
| Load | 50kVA, PF=0.85 |
| $Z_{sc}$ Injection transformer | 4% |
| DC link voltage | 500V |
| DVC energy storage | 75mF |
| Filter capacitor | 0.1mF |
| Filter inductance | 0.5mH |
| Converter switching frequency | 20kHz |

Obviously, the most severe fault is the one occurring immediately after the series unit at the moment which gives rise to the highest possible DC current component. Fig. 2 illustrates that this maximum transient short circuit current exceeds 50pu. Assuming only solid faults the least severe fault, occurring at the load-bus (end user) at the instant that results in zero DC current component the short circuit current exceeds 15pu. As shown in Fig. 2.

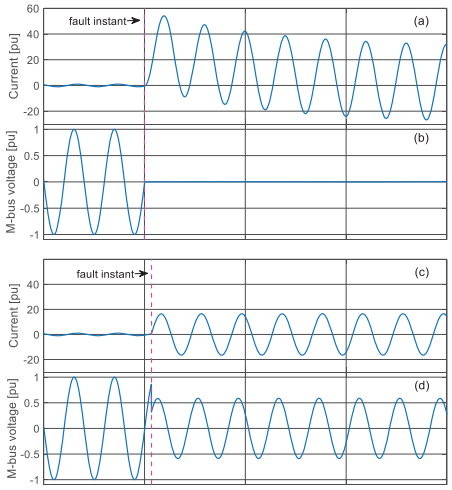


Figure 2 (a) Maximum short circuit current, (b) M-bus voltage for max case, (c) Minimum short circuit current, (d) M-bus voltage for minimum case.

### *A. Circuit breaker*

Using the fault calculation results for the maximum and minimum short circuit current and compatible with protection coordination of the grid, the upstream circuit breaker (CB) would be adjusted. The CB tripping curve is illustrated in Fig. 3. Therefore, the instantaneous tripping unit of the CB can be set on a value between 5 to 10 times the rated current.

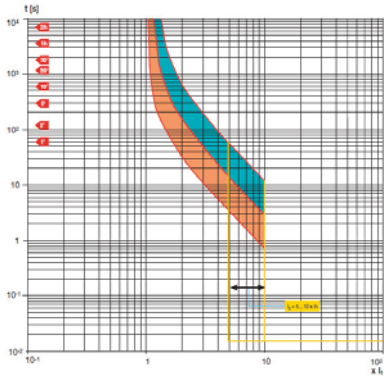

Figure 3 Tripping curve of the circuit breaker (CB)

Referring to the fault analysis results in Fig. 2, a solid fault at any point downstream the circuit breaker can be detected instantly by this CB setting. Moreover, according to the CB datasheet, it is supposed to break the short circuit current in less than 10 cycles (maximum 200ms).

## III. PASSIVE FAULT CURRENT LIMITING STRATEGY

The passive FCL strategies are described as A, B and C in the following.

### *A. Strategy A - FCL through injection transformer*

This protection strategy is proposed in literatures for integrating an FCL function into series devices. In [3] and [10] an integrated protection scheme with varistors, thyristors and mechanical or thyristors by-pass is proposed.

The configuration of this strategy is depicted in Fig. 4, in several protection schemes thyristors are intended to take over the current for the power electronic converters during overload or fault situations.

The operation principle is explained in the following steps: as soon as fault is detected, zero-state condition (no gate drive signal) is applied to the converter. The IGBTs are supposed to tolerate the flow of short circuit current (in terms of both electromagnetic forces and also thermal limitations) for some micro seconds prior to realization of FCL function, thereafter the control system turns on $SS_1$. $SS_1$ reacts fast and by taking advantage of short circuit impedance of injection transformer, which is saturated during short circuit, limits the fault current considerably. Varistors as a voltage dependent resistance, can be used to detect and limit voltage spikes across the DVC but cannot ensure a continuous current path. Varistors must effectively be placed at the secondary side of the injection transformers.

Considering a non-solid fault, when the fault current is not of a high value, the FCL function may postpone the tripping operation of the circuit breaker, which causes a long-term voltage sag to the parallel loads. Therefore, avoiding this condition, a mechanical or thyristors by-pass as $SS_3$ integration is necessary. When the fault current is too low, the control system fires $SS_3$ to increase the short circuit current so the fault can be detected quickly.

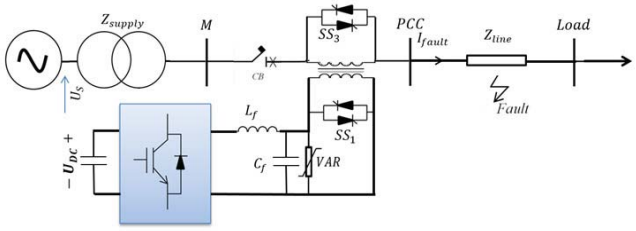


Figure 4 FCL operation through injection transformer (Strategy A)

This approach gives the benefits of simplicity in control system and the least required oversizing and number of auxiliary equipment. However, a survey into the general values of short circuit impedance of the injection transformer and distribution feeder standard impedances illustrates that current limitation for the faults adjacent to the series unit is not highly effective through this strategy.

### *B. Strategy B - FCL through filter inductance*

The configuration of this strategy is depicted in Fig. 5 and analyzed in [9]. The $SS_1$ is moved in front of the DVC converter, so any over voltage cannot be affecting the DVC inverter.

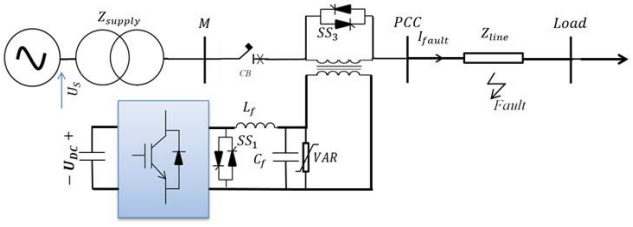


Figure 5 FCL operation through filter inductance (Strategy B)

Encountering a fault condition, the control system turns off the converter and closes the $SS_1$. Therefore, the filter capacitor and inductor become parallel and their equivalent impedance is added to the impedance of the injection transformer in the current path. The short circuit current flows almost completely (neglecting resonance between the capacitor and the inductor and the effect of transformer saturation) through the inductor of the filter. The reason is that $X_{inductor} << X_{capacitor}$.

Integration logic and functionality of by-pass $SS_3$ is the same as it is explained within strategy A.

### *C. Strategy C - Three-level merged FCL strategy*

Another passive FCL function is depicted in Fig. 6. An external small inductance, $L_{FCL}$, in series connection with the anti-parallel thyritors $SS_1$ is inserted into the device to improve the performance.

The principle of operation is explained in this way: following the fault detection, the control system puts the DVC converter in zero-state and turns the static switch $SS_1$ on to limit the short circuit current, however, the line current is continuously sensed and compared with the minimum circuit breaker setting. If the short circuit current following a solid fault violates the safety margin for the minimum circuit breaker instantaneous tripping point, the static switch $SS_2$ is fired. As last step when the fault current is not of a high value, the control system fires $SS_3$ to by-pass the device and its functionality is same as previous case.

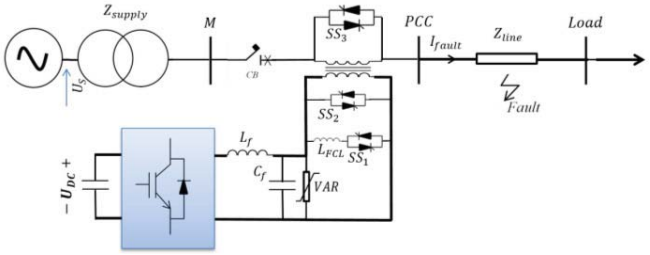


Figure 6 Three-level merged FCL strategy (Strategy C)

## IV. Active Fault Current Limiting Strategy

Active FLC strategies as D and E, are based on controlling DVC inverter actively to inject an appropriate voltage into the faulted feeder for the aim of limiting the short circuit current.

To implement an active FCL strategy in a single phase DVC converter it is necessary to implement a control scheme as shown in Fig. 7 [8]. Fault detection procedure is performed through measuring the current rate of rise and comparing it with a pre-set value. As soon as fault is detected, the reference generator providing the DVC voltage control loop with an appropriate $U_{DVC,ref}$ in correspondence with $K_{CB}$. The inner loop controls the filter capacitor current in order to regulate output voltage of the DVC during transient operation.

In addition, in order to detect recovery from the downstream fault, the voltage variation of PCC-bus (load side of the DVC injection transformer) is employed. Following the fault clearance, this voltage will increase, once it is restored to a preset threshold level, the FCL function of the DVC could be terminated. Active FCL strategies can be implemented in impedance and reactance modes.

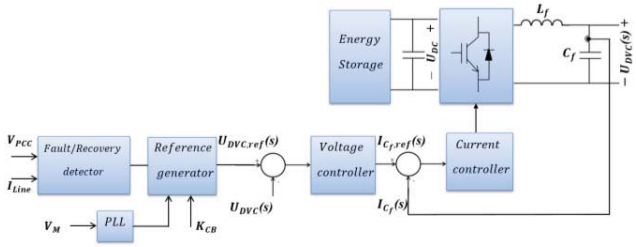


Figure 7 DVC control scheme active FCL function (Strategy D and E)

### *A. Strategy D - FCL strategy active impedance*

If a fault occurs when the DVC injects a voltage phasor in phase with feeder voltage drop, the DVC acts as an active impedance $Z_0$ whose $R/X$ ratio is the same as feeder impedance to the faulted point [7]. The control scheme is the same as it is depicted in Fig. 7, but the generated reference voltage for DVC converter is in phase with upstream M-bus voltage. This strategy gives the minimum requirement for DVC voltage injection capability; however, it causes DC link voltage rise due to absorbing real power during FCL mode.

### *B. Strategy E - FCL strategy active reactance*

Controlling the DVC as active inductor could ensure zero real power absorption during FCL mode thus avoids DC link voltage increase. In this case the voltage injection of the DVC is higher than Strategy D and if it is not critical point, this strategy can be more interesting. For this purpose, a constant active reactance injection of $X_0$ using flux-charge control scheme has been treated in [6].

## V. Considerations on Proposed FCL Strategies

It is important to underline that introducing any series device into a feeder could imply a revision on protection coordination of all upstream circuit breakers settings. Sometimes this modification may give rise to a complicated issue. Moreover, in order to guarantee the minimum tripping operation of the circuit breaker and to protect the DVC device, a mechanical or static switch $SS_3$ to by-pass it, has to be always implemented, but DVC converter and other components sizing should be as low as possible due to economic reasons. Integrating a passive FCL function (strategies A, B, C), it is possible to decrease the DVC size. Doing so, the initial cost can be reduced even if adding any new components (as SS and L) will increase the initial costs. Active FCL strategies (D and E) need implementation of control logic only. They do not need any integration of extra components. Moreover, a communication channel between DVC and upstream circuit breaker could be evaluated to improve upstream M-bus voltage restoration during fault condition adopting FCL strategies. Feasibility and reliability of such communication channel is a matter of concern by this time. Apart from DVC converter and components size, the reliability, robustness and the speed response are the main evaluation criteria to compare different strategies.

## VI. Simulation Results and Discussion

In order to have a comparison indication for studying FCL performance of addressed topologies and control scenarios throughout this paper, the simulation results done using in MATLAB environment for each treated FCL approach are presented in this section. For the simulation, the radial low voltage distribution network reported in Fig. 1 is considered to include DVC series devices as reported in Fig. 4, Fig. 5 and Fig. 6, the parameters used for the simulation are given in Table I.

Referring to considered fault incidents. In this section, two fault types are applied in the following simulations at time instant 0.2s and 0.204s for short circuit at PCC and load bus respectively (due to the network conditions those values give the highest short circuit current). In order to observe the behavior of the network during FCL mode, it is assumed that there is no breaking operation of upstream circuit breaker before 0.35s.

### *A. Result Strategy A*

Simulation results for FCL operation through injection transformer is treated in Fig. 8 for the most severe solid fault and for the least severe solid fault. Considering the current waveform, the limitation imposed on the most severe solid fault is not sufficient as the first peak of short circuit current touches 25pu with the steady state value of 15pu, and a deep voltage sag of 50% is expected.

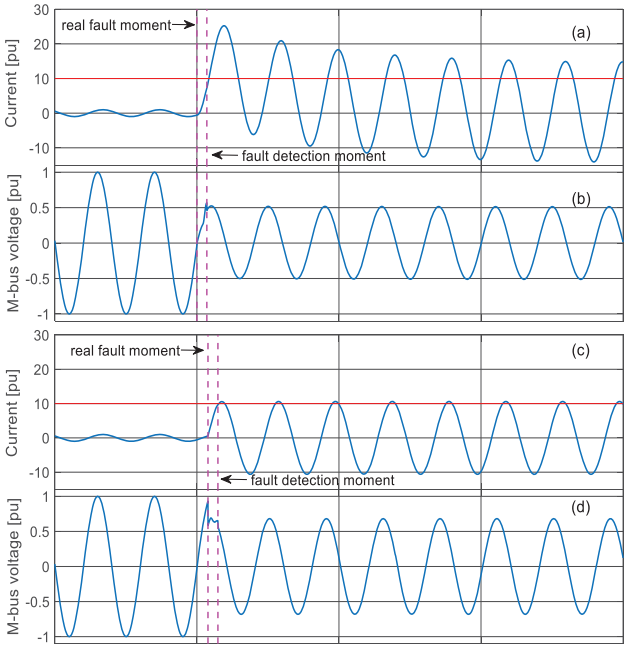


Figure 8 FCL strategy A for the most severe solid fault, (a) line current, (b) M-bus voltage, and for the least severe solid fault, (c) line current, (d) M-bus voltage

Even though the FCL performance of this strategy for the fault at PCC is not highly effective, for the fault at the end user it is completely effective such that more limitation gives rise to interference with upstream circuit breaker, which have to be avoided. An increasing of injection transformer short circuit impedance cannot be an option to make passive FCL solution of strategy A more effective. Indeed, it could cause higher voltage drop and losses during normal operation of the DVC and, there is also the possibility of interference with the upstream protection devices especially for faults close to the end of the feeder. So, the value reported in Table 1 can be

considered as limit value.

### *B. Result Strategy B*

FCL operation through filter inductance is simulated for the most severe solid fault and the results are depicted in Fig. 9. As a result of high value of the filter inductance the imposed strong limitation on the short circuit current can interfere with the circuit breaker set to $K_{CB}$=10. In addition, due to the high ratio of the filter inductance with respect to resistive part of the faulted circuit the ratio of the faulted feeder *X/R* becomes high, which gives rise to slow decaying DC component of short circuit current. Therefore, using this strategy postpones the first zero crossing of short circuit current.

It is possible to observe in Fig. 9, that in most severe solid fault, even if the first peak of short circuit current touches 15pu and the deep voltage sag reaches only 75%, the first zero crossing of the line current occurs at 6$^{th}$ cycle after the fault. This issue results in considerable increase of the let trough energy $I^2t$ that puts a high stress on upstream equipment including the circuit breaker, which reduces the device lifetime.

Indeed, in the case of load bus fault, the peak of short circuit current is strongly reduced interfering with the circuit breaker setting. Moreover, due to resonance phenomenon between the filter capacitor and the inductance of the circuit the M-bus voltage is polluted with harmonic contents.

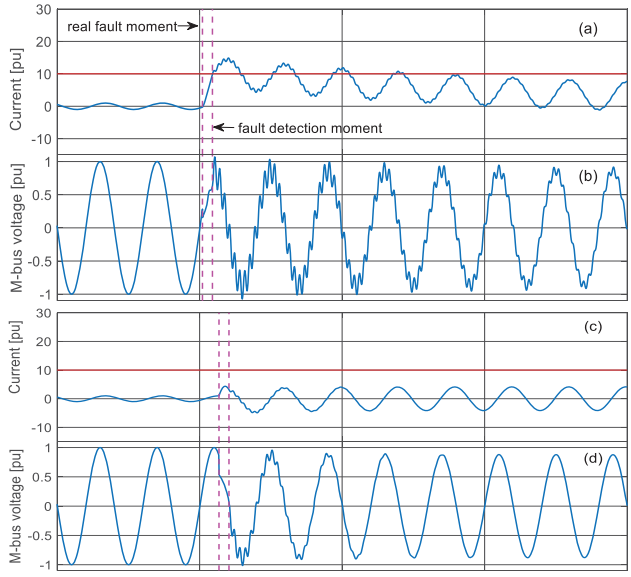


Figure 9 FCL Strategy B for the most severe solid fault, (a) line current, (b) M-bus voltage, and for the least severe solid fault, (c) line current, (d) M-bus voltage

### *C. Result Strategy C*

Simulation results for the FCL strategy C with the assumption of $K_{CB}$=10 are treated in Fig. 10 for the most severe solid fault and the least severe solid fault.

As it is observed thanks to fault current limiter inductance $L_{FCL}$ the most severe solid fault is effectively limited to 10pu and the M-bus voltage is restored to 65%. Since the limited short circuit current does not violate the safety margin of upstream circuit breaker only $SS_1$ is fired during FCL mode.

For the fault at the load-bus, the limitation provided by $L_{FCL}$ violates the safety margin of instantaneous operation point of the upstream CB, therefore the control system fires the $SS_2$ after one cycle. As a result, the short circuit current is effectively limited while avoids interfering with protection coordination.

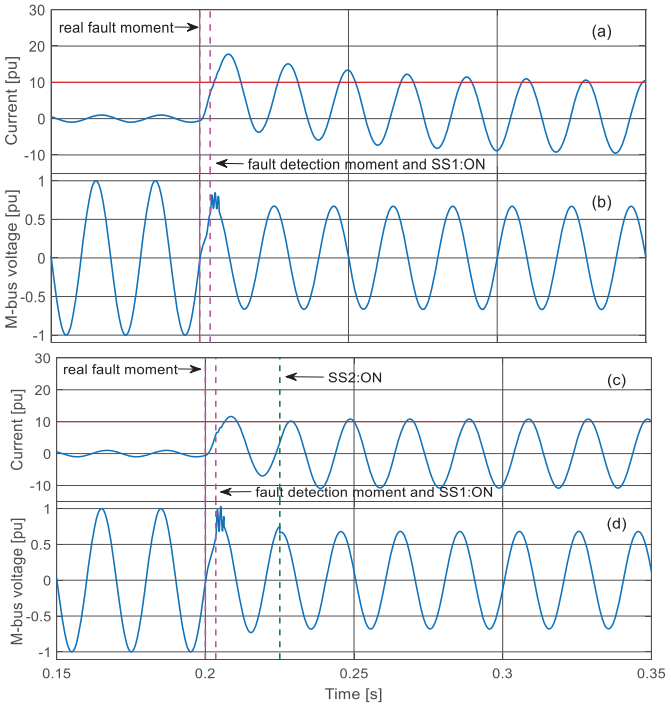


Figure 10 FLC strategy C for the most severe solid fault, (a) line current, (b) M-bus voltage, and for the least severe solid fault, (c) line current, (d) M-bus voltage

### *D. Result Strategy D*

This active strategy involves DVC converter in FCL operation in order to keep the short circuit current, as close as possible, to 10pu.

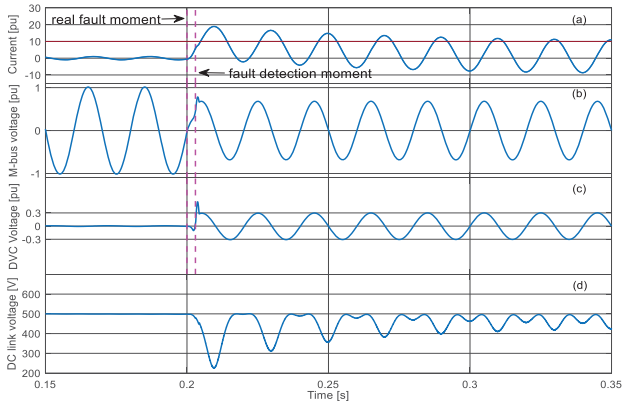


Figure 11 FCL strategy D (a) line current, (b) M-bus voltage, (c) DVC injected voltage, (d) DC link voltage

Therefore, doing, the M-bus voltage is recovered to more than 65% and the DVR injected voltage is 30%. Even if with this strategy the DC link voltage changes and it is important to

consider it during FCL mode. This strategy suffers from DC link voltage increment during fault due to real power absorption. Even if the absorbed power is not very high due to the low voltage of the DVR and the poor power factor in the faulted feeder, the DC link voltage variation is significant during short-term FCL mode as shown in Fig. 11.

### *E. Result Strategy E*

In order to compare the performance of active inductance FCL mode with active impedance (Strategy D), the simulation results of Strategy E are depicted in Fig. 12. As it can be observed the results in this case are better, there is 5% increment in voltage injection requirement of the DVC. The reason is originated from dominantly inductive nature of the faulted circuit in the considered network.

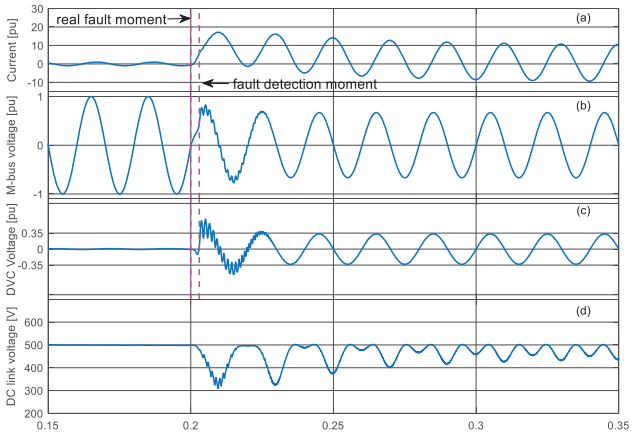


Figure 12 FCL strategy E (a) line current, (b) M-bus voltage, (c) DVC injected voltage, (d) DC link voltage

### *F. Final considerations*

In order to improve upstream M-bus voltage restoration during fault, an FCL strategy has to be followed. Limit the current to $K_{CB}$=10 cannot permit a good restoration because the M-bus voltage, can reach to 65% only. Therefore, only adopting FCL strategies able to limit the fault current to/close to the line/load nominal current. For this purpose, a communication channel between DVC and upstream circuit breaker should be established. Once the DVC goes into FCL mode, it informs the upstream circuit breaker, so the instantaneous current breaking is still achievable [8].

Employing communication-less approach in active FCL strategies, decreases the required voltage injection capability of the DVC but the DVC should be sized to handle the high short circuit current before the CB tripping time (around 10 cycles).

## VII. Conclusions

The comprehensive and judicious comparison of the treated FCL strategies in this paper requires performing a dedicated case study for the target network.

For this purpose, some benchmarks and criteria are required. These criteria include the required sizing power of the DVC equipped with FCL function, the required voltage injection capability for the FCL function, prerequisite of a communication channel, complexity of the control system, let-through energy before tripping operation, DC-link voltage increment during FCL mode and the effect of the FCL function upon the total reliability of the network.

Integrating FCL function into a DVC is possible through rated FCL and communication less FCL approaches. While the rated FCL approach give the benefit of complete restoration of upstream bus voltage and have the capability of avoiding phase jump for parallel loads, they suffer from prerequisite of installing reliable communication channel and comparing to DVC primary duty as a voltage compensator they result in oversizing DVC to the rated power of downstream load.

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