Operation and Efficiency Analysis of a 5-level Single-Phase Hybrid Si/SiC Active Neutral Point Clamped Converter

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Mohammad Najjar, *Student Member, IEEE,* Mahdi Shahparasti, *Senior Member*, *IEEE,* Alireza Kouchaki, *Member, IEEE,* Morten Nymand, *Member, IEEE*

***Abstract*—The ability to improve both the size and efficiency of multilevel single-phase converters is a key to uplift them as an attractive solution for industries, while the high number of switches and complex modulation techniques understandably make them unattractive. 5-level active neutral point clamped converter, due to its inherent advantages such as employing different switching frequencies and using different switch technologies, presents an ideal candidate for study. This paper performs a comprehensive analysis of the converter to highlight the advantages of it. This analysis results in a modified hybrid modulation that effectively regulates the neutral point (NP) of the dc-link. Consequently, the combination of the topology and the modified modulation make the converter ideal to utilize two different switch technologies- in this paper Silicon Carbide (SiC) and Si MOSFET. To evaluate the analysis and the effectiveness of modulation, a 2kW hybrid 5-level ANPC is built. Analyzing of the behavior of the converter current, power loss in the filter and switches are, therefore, calculated. The efficiency measurement is performed and compared with the calculated efficiency. There is a close coherency between the measurement and the calculated results and a peak efficiency of 98.4% is achieved.**

***Index Terms*—Single phase, Efficiency, SiC metal oxide semiconductor field effect transistor (MOSFET), Five-level inverter, Space vector pulse width modulation.**

I. Introduction

Multi-level converters (MLCs) have gained more attraction in power electronic applications due to their superior characteristics such as lower *dv/dt*, improved current and voltage total harmonic distortion (THD) and smaller filter size compared with conventional converters [1], [2]. Increasing the number of output voltage levels requires more semiconductors, which corresponds to system complexity and higher cost. However, by focusing on efficiency and achieving smaller filtering (due to higher number of output voltage levels), single-phase multilevel topologies can still be interesting.

Among various topologies that are presented for single-phase multilevel topology, the 5-level neutral-point-clamped (5L-NPC) converter is an interesting topology [3], owing to the fact that it presents high efficiency and compact design and can generate up to five output voltage levels [4]. Fig. 1 presents eight well-known 5-level single-phase NPC based structures. Fig. 1(a) shows a 5 level MLC based on basic H-bridge NPC converter or symmetrical NPC [4]–[7]. In this topology, two 3-level NPC converters with 8 switches and 4 diodes are utilized to produce a 5-level output voltage. By replacing the diodes with active switches in the NPC structure, extra output vectors can be obtained. Consequently, these vectors can be employed to control the NP voltage and to distribute losses among power switches. Therefore, the 5L-NPC can be modified to an ANPC based structure, as it is shown in Fig. 1(b). The high number of semiconductors counts is the main drawback of this topology. To solve this issue, a 5L-ANPC with a coupled inductor is presented in [8], which eight power switches are employed (Fig. 1(c)). However, the coupled inductors reduce the system efficiency due to the circulating current [9]. A flying capacitor-based ANPC converter was presented in [8], where a flying capacitor is located between the high-voltage and the low-voltage stages (Fig. 1(d)). As it can be seen from Fig. 1(e), a single-phase asymmetrical NPC topology was proposed in [10] with the ability to provide five voltage levels. This topology is composed of a 3L-NPC and a 2-level half-bridge legs. Thus, two switches and two diodes are saved compared to symmetrical NPC topology in Fig. 1(a). However, an external circuit is applied to balance the voltages of the dc-link capacitors. According to Fig. 1(f), if both diodes are replaced with active switches in asymmetrical 5-level NPC (Fig. 1(e)), a new ANPC asymmetrical converter can be obtained [11], [12]. In this converter, 2 switches are operating at fundamental frequency [12]. Fig. 1(g) shows a 5-level reduced switches converter, wherein the second leg is in parallel with the middle switches on 3L-NPC in the first leg [13], [14]. All switches are modulated at the same switching frequency. If the diodes are replaced with active switches, another topology can be obtained (Fig. 1(h)) [3], which is the case under study in this paper. In this structure, eight switches are utilized, which compared to

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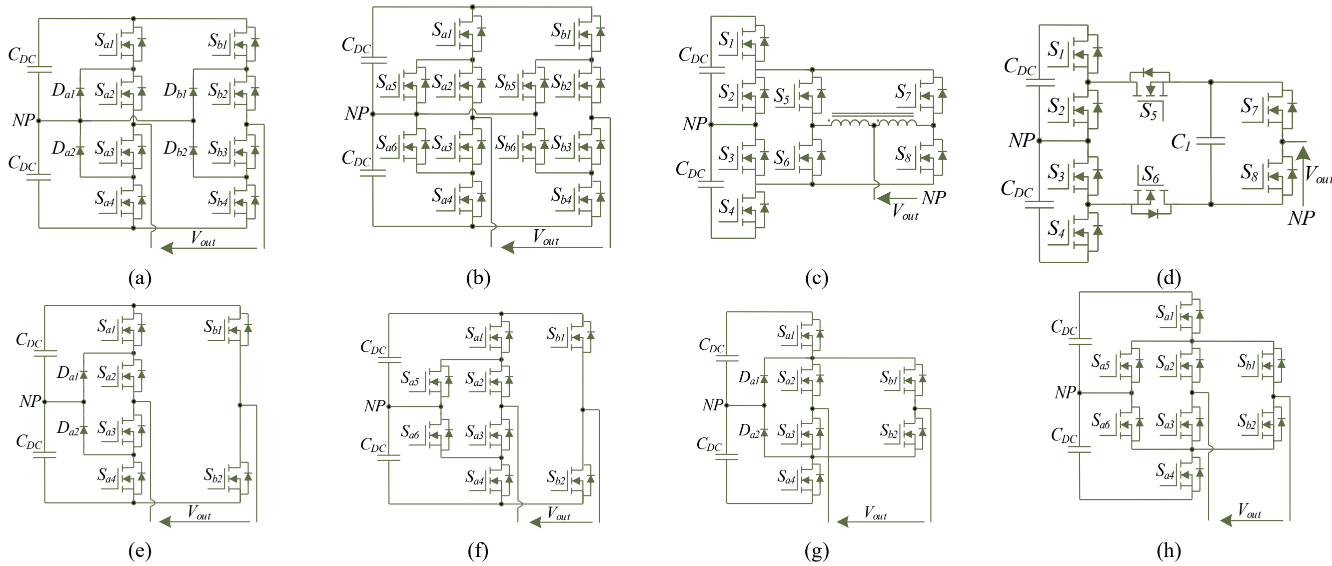


Fig. 1. The 5-level NPC based single-phase converters (a) symmetrical 5-level NPC (b) symmetrical 5-level ANPC (c) 5-level ANPC coupled inductors (d) 5-level ANPC flying capacitor (e) asymmetrical 5-level NPC type-1, (f) asymmetrical 5-level ANPC type-1 (g) asymmetrical 5-level NPC type-2, (h) asymmetrical 5-level ANPC type-2.

the symmetrical single-phase NPC structure (Fig. 1(a)) four diodes are saved. The other advantages of this topology are its flexibility in controlling the NP voltage and having a hybrid switching frequency.

A review of the literature reveals a focus on optimizing 5-level single-phase converters to obtain high efficiency [11], [12], [15]–[20]. By comparing the symmetrical 5-level NPC, asymmetrical 5-level NPC (Fig. 1(e)) and asymmetrical 5-level ANPC, it has been concluded in [11] that the ANPC converter has greater efficiency over the whole range of output power. Another comparison between 5L-NPC converters with different communication cells at the output has been done in [15], in which the converter with uncoupled inductors has higher efficiency compared to the one with an autotransformer. The converter efficiency in [15] at full load (5kW) is 96.2%. In [18], an asymmetrical T-type transformer-less inverter for PV applications has been presented, where a 3-level T-type leg is combined with a 2-level half-bridge leg to create a 5-level converter. Its efficiency reached less than 98% with the switching frequency of 16 kHz. A common ground inverter produces a 5-level output voltage with only six switches and two flying capacitors was proposed [20] but its efficiency is limited to 96.6%.

Most of the above solutions and structures are limited to the use of silicon devices and IGBTs. Meanwhile, the recent emergence of wide bandgap (WBG) devices, such as silicon carbide (SiC), offers a solution to improve the converter efficiency and power density. On the other hand, using these devices needs more detailed considerations towards design of the gate driver circuits, layouts and component selection. Therefore, a topology with the flexibility of employing various modulation techniques that accommodates both high and low frequency switches can simplify the design and at the same time utilizes the advantages of SiC MOSFETs. Different modulation techniques have been proposed for single-phase converters mainly based on carrier-based PWM (CBPWM) implementation [5], [21], [22] and space vector PWM (SVPWM) [6]. SVPWM in three and five segments provides more redundancy to choose the proper output vectors and consequently provides a better control option [23] [24]. Two hybrid SVPWMs for a single-phase three-level NPC are proposed in [6], [25] by introducing the weight coefficient of the redundant vectors which leads to optimizing high-order harmonic distribution and reducing the line current harmonics.

This paper presents the efficiency analysis of the asymmetrical 5-level ANPC as shown in Fig. 1(h). This topology allows the use of hybrid modulation technique, which can be employed to improve the efficiency of the converter. As a result, the devices are chosen from different semiconductor technologies. A modified hybrid space vector modulation (SVM) technique is used to generate high-quality output voltage, in which through the employment of a weight coefficient for redundant vectors, the NP voltage of the converter is also regulated. To achieve a complete efficiency analysis of the converter, the root mean square (RMS) current of each switch and dc-link capacitor are analyzed. Semiconductor switch losses of high frequency switches are determined by analyzing the switching states and using calculated RMS values. To evaluate the calculated efficiency, a 2 kW SiC/Si MOSFETs based converter is constructed and the analyses are compared with various experimental results.

In summary, the main contributions to this paper can be listed as follows:

1) Hybrid employment of SiC/Si switches in the structure of the converter.

2) Developing a hybrid SVM technique with a weight factor in which the NP voltage balancing is embedded.

3) Comprehensive loss analysis of the converter, which includes the calculation of the RMS current of different switches and the dc-link capacitor.

4) Studying the effects of weight factor on the converter efficiency, dynamic response of the NP voltage balancing system, magnitude of output harmonics and current ripple in the filter inductor.

The rest of the paper is organized as follows. The converter structure and switching states are presented in section II. Section III presents the modified hybrid SVM technique. The semiconductor selection and loss analysis are investigated in section IV. The experimental results are demonstrated in section V. Finally, section VI concludes the study.

II. Converter Structure and Switching States

The general structure of the converter is depicted in Fig. 2 [3]. The converter is composed of eight switches and two dc-link capacitors. Five different voltage levels can be obtained through 10 switching states, which are listed in TABLE I. In the positive half cycle, the dc-link voltage (V_{dc}) appears at the output when S_1, S_4, S_5 and S_8 are conducting (state P), Fig. 3(a). As shown in Fig. 3(b) and (c), half of the dc-link voltage ($0.5V_{dc}$) appears at the output with two switching states, when S_1, S_3, S_5 and S_8 (state HP$^+$) or S_2, S_4, S_5 and S_8 (state HP$^-$) are in turn-on condition. In HP$^+$, the voltage of the upper dc-link capacitor (V_{dc1}) appears at the output; while, the output voltage is equal to the voltage of the lower dc-link capacitor (V_{dc2}) in HP$^-$. This redundancy (Redundancy I), which generates half of the dc-link voltage at the output, can be used for controlling the NP voltage. There are four sets of combinations (states OS$^+$, OS$^-$, OL$^+$ and OL$^-$) to produce a zero-voltage level at the output. The difference between these states is the number of switches in the path of the current. For switching states of OS$^+$ and OS$^-$, the current closes its path through two switches, S_5 and S_7 or S_6 and S_8, respectively. While, four switches are conducting to generate a zero-voltage level in OL$^+$ and OL$^-$ states. In these two states (OL$^+$, OL$^-$), S_2 and S_3 are in the on-state and the combinations of either S_5 and S_8 or S_6 and S_7 provide zero voltage (see Fig. 3(d) and (e)). Consequently, another redundancy is introduced (Redundancy II) through OL$^+$ and OL$^-$, which can be used to achieve a hybrid modulation technique. In the negative half cycle, the switching conditions of S_1- S_4 for different states (N, HN$^+$ and HN$^-$) are similar to their counterparts in the positive half cycle (P, HP$^+$ and HP$^-$) and the states of S_5, S_6, S_7 and S_8 are complementary. These output vectors are shown in Fig. 3(f)- (h).

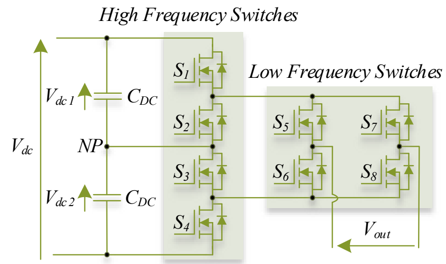


Fig. 2. The structure of 5-level switch reduced single-phase ANPC.

TABLE I
The switching states of 5-level single phase ANPC

Output States	Output Voltage	Switching states							
		S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
P	V_{dc}	1	0	0	1	1	0	0	1
HP$^+$	$V_{dc}/2$	1	0	1	0	1	0	0	1
HP$^-$	$V_{dc}/2$	0	1	0	1	1	0	0	1
OS$^+$	0	*	*	*	*	1	0	1	0
OL$^+$	0	0	1	1	0	1	0	0	1
OL$^-$	0	0	1	1	0	0	1	1	0
OS$^-$	0	*	*	*	*	0	1	0	1
HN$^+$	$-V_{dc}/2$	1	0	1	0	0	1	1	0
HN$^-$	$-V_{dc}/2$	0	1	0	1	0	1	1	0
N	$-V_{dc}$	1	0	0	1	0	1	1	0

The Redundancy II is employed to achieve hybrid modulation in which 4 switches (S_5-S_8, LF switches) are switched at low frequency (grid frequency) and the rest (S_1 - S_4, HF switches) operate at high switching frequency. Therefore, among all zero combinations, just two of the zero states (OL$^+$ and OL$^-$) are utilized. The disadvantage of using these two vectors is that there are four switches in the path of current and consequently, the conduction loss of the converter is increased. On the other hand, during zero crossing, S_2 and S_3 are kept on, which makes the voltage across S_5, S_6, S_7 and S_8 becomes almost zero. As a result, zero voltage switching (ZVS) is achieved. The main losses in LF switches are related to conduction and output capacitive losses. The output capacitive losses are related to the charge and discharge of the output switch capacitor.

The voltage across LF switches is the full dc-link voltage whenever the converter is switching at P and N states. For HF

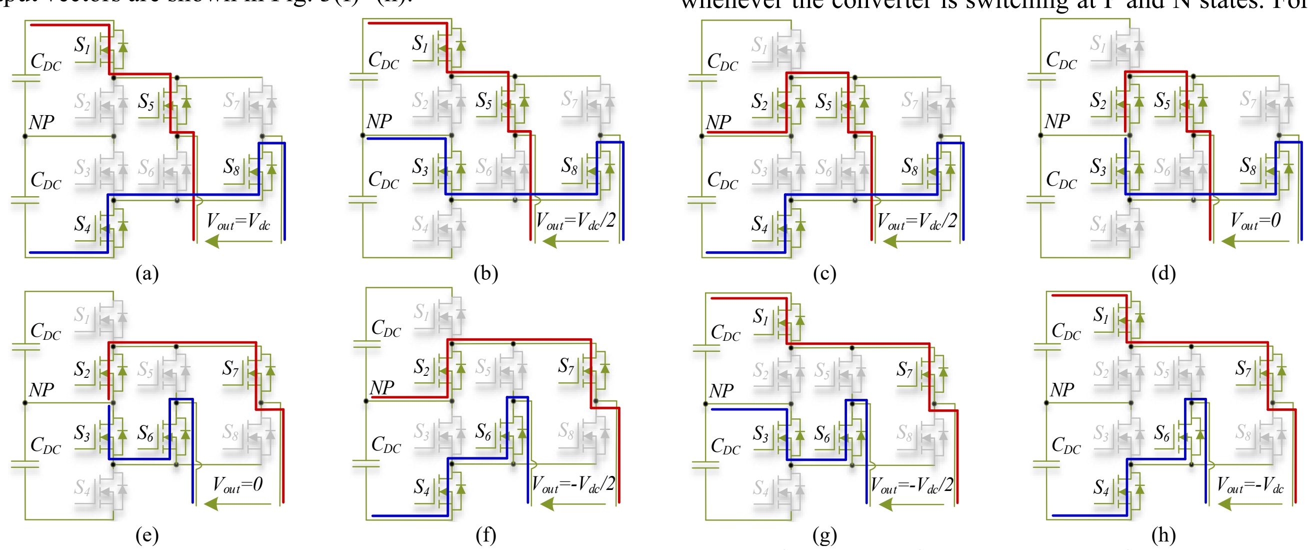


Fig. 3. The output vectors of hybrid switch reduced single-phase ANPC converters (a) P (b) HP$^+$ (c) HP$^-$ (d) OL$^+$ (e) OL$^-$ (f) HN$^-$ (g) HN$^+$ (h) N.

TABLE II
The condition and duty times of different sectors

Sector	1	2	3	4
Condition	V_{ref}>0.5	V_{ref}>0 & V_{ref}<0.5	V_{ref}<0 & V_{ref}>-0.5	V_{ref}<-0.5
t_a	T_{sw}-t_b	T_{sw}-t_b	T_{sw}-t_b	T_{sw}-t_b
t_b	2×(V_{ref}-0.5)×T_{sw}	2×V_{ref}×T_{sw}	2×|V_{ref}|×T_{sw}	2×|(V_{ref}+0.5)|×T_{sw}

TABLE III
The space vector sequence of different sectors

Sector	Voltages of the dc-link capacitors	Current sign	Switching sequence
1	v_{dc1}>v_{dc2}	i_c>0	P-HP^{+*}-P-HP^{-**}-P
		i_c<0	P-HP^{+**}-P-HP^{-*}-P
	v_{dc2}>v_{dc1}	i_c>0	P-HP^{+**}-P-HP^{-*}-P
		i_c<0	P-HP^{+*}-P-HP^{-**}-P
2	v_{dc1}>v_{dc2}	i_c>0	OL^{+}-HP^{+*}- OL^{+}-HP^{-**}- OL^{+}
		i_c<0	OL^{+}-HP^{+**}- OL^{+}-HP^{-*}- OL^{+}
	v_{dc2}>v_{dc1}	i_c>0	OL^{+}-HP^{+**}- OL^{+}-HP^{-*}- OL^{+}
		i_c<0	OL^{+}-HP^{+*}- OL^{+}-HP^{-**}- OL^{+}
3	V_{dc1}>V_{dc2}	i_c>0	OL^{-}-HN^{+**}- OL^{-}-HN^{-*}- OL^{-}
		i_c<0	OL^{--}-HN^{+*}- OL^{-}-HN^{-**}- OL^{-}
	v_{dc2}>v_{dc1}	i_c>0	OL^{-}-HN^{+*}- OL^{-}-HN^{-**}- OL^{-}
		i_c<0	OL^{-}-HN^{+**}- OL^{-}-HN^{-*}- OL^{-}
4	v_{dc1}>v_{dc2}	i_c>0	N-HN^{+**}-N-HN^{-*}-N
		i_c<0	N-HN^{+*}-N-HN^{-**}-N
	v_{dc2}>v_{dc1}	i_c>0	N-HN^{+*}-N-HN^{-**}-N
		i_c<0	N-HN^{+**}-N-HN^{-*}-N

*the time period equals to t_{s1}
** the time period equals to t_{s2}

switches, the blocking voltage is half of the dc-link voltage.

III. Modified Hybrid Space Vector Modulation for Single-Phase ANPC

In this section, a modified hybrid SVM technique is proposed to regulate the dc-link voltage of the capacitors. The vector diagram for a single phase 5-level converter is shown in Fig. 4. The vector diagram is divided into four sectors. Among 10 different vectors (TABLE I), two of these vectors are large vectors and four are zero vectors. The large and zero vectors do not have any influence on the NP voltage balancing. However, the small vectors (HP$^+$, HP$^-$, HN$^+$ and HN$^-$) can change the NP voltage. The reason is that the current closes its path through one of the dc-link capacitors. In all sectors, there is a pair of small vectors which provide a degree of freedom to control the NP voltage.

The reference voltage is defined as follows:

$$V_{ref} = m \times \cos(\omega t + \varphi) \tag{1}$$

where ωt is the angular frequency, φ is the position of reference vector and m is the modulation index as follows:

$$m = \frac{V_{ac} \times \sqrt{2}}{V_{dc}} \tag{2}$$

where V_{ac} is the RMS of the output voltage and V_{dc} is the voltage of the dc-link (V_{dc1}+V_{dc2}).

In the suggested method, the reference voltage is synthesized with all vectors in each section. For example, vector P and both small vectors of HN$^+$ or HN$^-$ are utilized in sector 1. TABLE II specifies the true condition for each sector and the applied time of each vector. T_{sw}=$1/f_{sw}$ is the switching period and t_a and t_b are

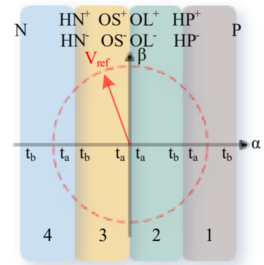


Fig. 4. The space vector diagram of single-phase 5-level converter.

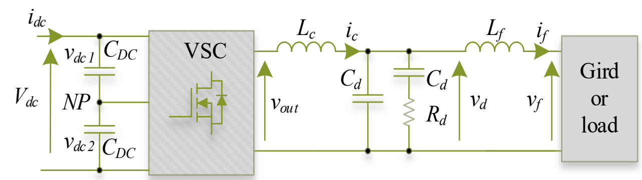


Fig. 5. The schematic of the system.

duty times of applied vectors, as can be seen in Fig. 4. The duty times of small pair vectors can be different. In fact, the NP voltage can be controlled by changing the duty time of these small pair vectors. The reason is that the output current flows through one of the dc-link capacitors for a longer time than the other. Defining a weight coefficient as n, the periods of small pair vectors can be divided into different values which are defined as follows:

$$\begin{aligned} t_{s1} &= n \times T_s \\ t_{s2} &= (1-n) \times T_s \qquad 0.5 \le n \le 1 \end{aligned} \tag{3}$$

where T_s is the time period of small pair vector which can be obtained from TABLE II, t_{s1} and t_{s2} are the time periods of two pair vectors.

To control the NP voltage, the voltages of the dc-link capacitors and the output current are monitored in each switching cycle and proper vectors are selected and applied. The whole sequence for all sectors is listed in TABLE III.

The value of n defines the dynamic of the system to regulate the voltage of the dc-link capacitors, i.e. larger n means faster dynamic. For bipolar dc-link applications or when the load uses the NP connection, the controller can employ n for unbalanced loads. However, in this condition, the losses of high-frequency cells become unequal. In the case n=0.5, the output will be the same as carrier-based PWM (CBPWM) [26], [27]. It means that the effective frequency of the output voltage is two times larger than the switching frequency. If the value of n is equal to one, during each switching cycle, just one of the small pair vectors is utilized. Consequently, the effective frequency of the output voltage is equal to the switching frequency.

By utilizing the output current condition and the value of n, this method is capable of controlling the NP voltage at different power factors and modulation indexes.

IV. Hardware Design and Efficiency Analysis

A. LCL filter design and components selection

To demonstrate the performance of the converter and hybrid SVM, a prototype is implemented. The schematic of the system is shown in Fig. 5. The filter is comprised of a converter side

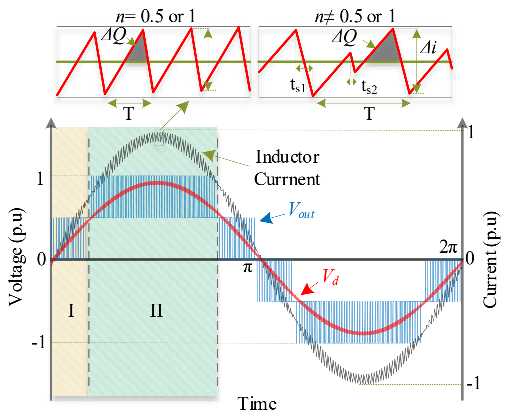


Fig. 6. The current ripple behavior of the converter side inductor.

inductor (L_c), a grid side inductor (L_f) and a shunt capacitor (C_d). L_c can be designed based on the maximum acceptable current ripple, which is normally adjusted to be between 5 up to 30 percent of the peak-to-peak of nominal current. If the filter is designed correctly, the major current ripple occurs in L_c. In addition, it is assumed that the voltage after L_c is sinusoidal [28]. As a result, the voltage across L_c can be calculated as follows:

$$v_{Lc}(t) = v_{out}(t) - v_d(t) \quad (4)$$

Each half cycle is comprised of two sectors. Therefore, the general current ripple (Δi_c) behavior in L_c can be split into two distinct regions, as illustrated in Fig. 6. (I and II).

Based on the time periods of TABLE II, the current ripple and maximum current ripple, with consideration of n value, can be represented as follows:

$$\begin{aligned} &\Delta i_c = \frac{2nV_{dc}}{f_{sw}L_c}(0.5 - m\sin(\omega t))m\sin(\omega t) && \text{Region I} \\ &\Delta i_c = \frac{2nV_{dc}}{f_{sw}L_c}(1 - m\sin(\omega t))(m\sin(\omega t) - 0.5) && \text{Region II} \quad (5) \\ &\Delta i_{\max} = \frac{nV_{dc}}{8 f_{sw}L_c} \quad 0.5 \le \mathrm{n} \le 1 \end{aligned}$$

Considering (5), the current ripple when n=1 is two times larger than n=0.5. In addition, the minimum value of L_c can be calculated to reach the considered maximum current ripple.

Normally, the high frequency current ripple passes through the filter capacitor [28]. Thus, the minimum necessary capacitance (C_d) value can be determined by calculating the maximum converter current ripple. The maximum voltage ripple (ΔV_{ripple}) in the filter capacitor can be calculated as follows:

$$\Delta V_{ripple} = \frac{\Delta Q_{\max}}{C_d} \approx \frac{1}{C_d}\frac{1}{2}\frac{\Delta i_{\max}}{2}\frac{T}{2} \quad (6)$$

where ΔQ represents the charge in the filter capacitor as the shaded area in Fig. 6.

As it is shown in Fig. 6, T is the value of one cycle of current ripple. For simplicity, to calculate ΔQ the time interval is considered half of T. Therefore, the minimum required value of C_d can be obtained as follows:

TABLE IV
The general system specifications

Parameters	Symbol	Value
The output power	P_{nom}	2 kW
dc-link voltage	V_{dc}	360 V
The ac voltage	V_f	230 V
The grid frequency	f_f	50 Hz
Switching frequency	f_{sw}	70 kHz
Converter side inductor	L_c	350 µH
Grid side inductor	L_f	250 µH
Filter capacitor	C_d	1 µF

TABLE V
The specifications of HF and LF switches

Switch	Manufacturer number	Voltage (V)	Current (A)	$R_{DS\text{-}on}$ @25°C (mΩ)	Output switch charge (nC) @180V
SiC	SCT3060AR	650	39	60	39
Si	IPZ65R065C7	700	33	65	398

$$\Delta V_{ripple} \approx \frac{1}{64}\frac{1}{C_d}\frac{n^2 V_{dc}}{L_c f_{sw}^{\ 2}} \rightarrow C_d > \frac{1}{64}\frac{1}{\Delta V_{ripple}}\frac{n^2 V_{dc}}{L_c f_{sw}^{\ 2}} \quad (7)$$

The value of L_f can be determined based on required attenuation for the current harmonics at switching frequency. The required attenuation can be defined based on grid standards (e.g. IEEE 519). When the converter is switching at high frequency, the major harmonics of the output current drop at high frequencies, such as f_{sw} or $2f_{sw}$. At high frequencies, the line impedance stabilization network (LISN) can provide a well-defined grid impedance, which can be utilized to have an optimum filter and repeatable measurements [28]. Thus, the output voltage harmonics can be calculated as a function of LISN resistance (R_{LISN}) as follows:

$$V_{out}(s) = \frac{2R_{LISN}V_{an}}{L_c L_f C_d s^3 + 2R_{LISN}L_c C_d s^2 + (L_c + L_f)s + 2R_{LISN}} \quad (8)$$

where V_{an} is the converter voltage harmonics at f_{sw} or $2f_{sw}$ based on the considered modulation techniques. Since V_{out} is defined based on the considered standard, the value of grid side inductance can be easily calculated.

The specifications of the converter and filter parameters are listed in TABLE IV. The filter parameters are calculated using n=1 which demonstrates the worst-case condition from the current harmonics point of view.

Concerning the properties of SiC MOSFETs and the structure of the converter, ROHM Semiconductor SCT3060AR, with a 4-pin in TO-247N package is utilized for HF switches. The switch characteristics are listed in TABLE V. Utilization of two different switch technologies with two different switching frequencies has formed a hybrid converter.

In order to calculate the efficiency of the converter, a theoretical power loss analysis will be carried out.

B. Modeling of the conduction losses

To find the conduction losses for the switches and the dc-link capacitors, the RMS current for each device should be calculated. To calculate the RMS current for each device, an analytical approach similar to [29] is utilized. To simplify, the current is assumed to be sinusoidal and the phase difference between the current and the voltage is θ. Fig. 7 shows the duty

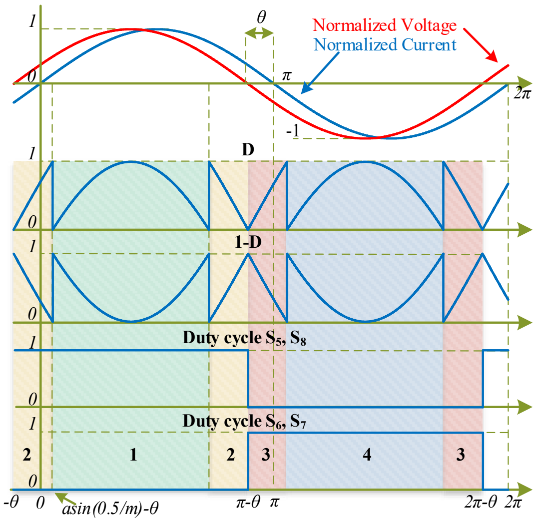


Fig. 7. The normalized voltage, current and the duty cycles [29].

cycles for high and low frequency switches. The modulation index represents the normalized voltage, which varies between zero and one. Due to the symmetrical operation of the converter, the RMS current of the top and bottom high-frequency switches can be considered equal. Also, the same condition is applied to the middle high-frequency switches.

The current is defined as:

$$i = I_p \sin(wt) \tag{9}$$

where I_p is the peak current. The RMS current of each switch can be calculated by following equation [29]:

$$I_{rms} = \sqrt{\frac{1}{T}\int_0^T \left[i(t)^2 \times D(t) \right] d(t)} \tag{10}$$

where *D(t)* is the effective duty cycle of the switch that can be found in Fig. 4, Fig. 7 and TABLE II.

For simplification, it is assumed that during the positive half-cycle, the voltage of the upper dc-link capacitor (HP^+), and during the negative half-cycle the lower dc-link capacitor voltage (HN^-) are used. In addition, n=1 is considered. By using equation (10), the RMS current of S_1 can be obtained as (11).

Employing the same procedure, the RMS current of S_2 is obtained as follows:

$$I_{rms\_S2} = I_p \sqrt{\frac{3\pi - 6m - 2m\cos 2\theta}{6\pi}} \tag{12}$$

Since LF switches are in turn-on state for half of the cycle, the related RMS current can be calculated as follows:

$$I_{rms\_LF} = \frac{I_p}{2} \tag{13}$$

The same procedure can be used to calculate the RMS current of the dc-link capacitor. The output current flows through one of the dc-link capacitors when a small vector is applied. For the upper dc-link capacitor, this happens whenever the small vectors of HP^+ and HN^+ are employed [see Fig. 3 (b) and (g)]. Considering the assumptions mentioned earlier, the upper dc-link capacitor can be in the current path during the positive half-cycle. As a result, by finding the RMS current of HP^+ vector during the positive half cycle, the RMS current of dc-link capacitors can be calculated as (14).

$$I_{rms\_cap} = I_p \sqrt{\frac{2m\cos(2\theta) - 6\arcsin\left(\frac{1}{2m}\right)}{6\pi} + \frac{\frac{\cos(2\theta)\sigma_1}{2m^2} + 6m - 6\sigma_1 + 3\pi}{6\pi} - \frac{2\cos(2\theta)\sigma_1}{6\pi}} \tag{14}$$

$$\sigma_1 = \sqrt{4M^2 - 1}$$

The conduction loss of each switch can be calculated using equations (11) - (14), and the turn-on resistor of each device can be obtained from its datasheet.

$$P_{con} = R_{ds-on} I_{rms}^{\ 2} \tag{15}$$

The body diode of SiC MOSFET has a very poor conduction characteristic. The body diode is conducting during the deadtime of the HF switches. In this work, the duration of deadtime is 120ns. Thus, the conduction loss related to the body diode is neglected. For Si MOSFETs, the gate signals of the conducting devices are always enabled to provide the current going through the channel. Thus, the conduction loss of the body diode for Si MOSFET is almost zero.

The same procedure can be performed to find the dc-link capacitors loss using equation (15). Instead of R_{ds-on}, the equivalent series resistance (ESR) of the capacitor should be replaced.

C. *Modeling of the Switching Losses*

The switching losses of HF switches can be divided into turn on (E_{on}) and turn off (E_{off}) losses. These losses can be extracted from datasheets, where both E_{on} and E_{off} are given individually for a single test condition, such as external gate resistors, gate voltage, drain-source voltage and drain current. Moreover, the reverse recovery of body diode is included in E_{on}. However, the conditions of the prototype and datasheet are different. Therefore, the parameters should be modified. In addition, the switch characteristics are obtained at an ambient temperature of 25°C. Meanwhile, the data can be employed for real test conditions because the temperature hardly affects the switching energies of the SiC MOSFET [30], [31]. Therefore, the temperature difference between the test and the datasheet is not

$$I_{rms\_S1} = \sqrt{\frac{1}{2\pi}\left[\begin{array}{l} \displaystyle\int_{-\theta}^{a\sin(0.5/m)-\theta} \left[i^2 \cdot (2m\sin(wt+\theta))\right] d(wt) + \int_{\pi-\theta-a\sin(0.5/m)}^{\pi-\theta} \left[i^2 \cdot (2m\sin(wt+\theta))\right] d(wt) + \int_{a\sin(0.5/m)-\theta}^{\pi-\theta-a\sin(0.5/m)} i^2 d(wt) + \\ \displaystyle\int_{\pi-\theta+a\sin(0.5/m)}^{2\pi-\theta-a\sin(0.5/m)} \left[i^2 \cdot (-2m(\sin(wt+\theta)+0.5))\right] d(wt) \end{array}\right]} \tag{11}$$

$$= I_p \sqrt{\frac{m(\cos 2\theta + 3)}{3\pi}}$$

included in the analysis. A modified relationship is developed to represent all the test conditions. The equations for E_{on} and E_{off} are expressed as follows:

$$E_{on-tets} = E_{on-datasheet} \cdot \frac{f_{Vds-on}(V_{ds-test})}{f_{Vds-on}(V_{ds-datasheet})} \cdot \frac{f_{id-on}(i_{d-test})}{f_{id-on}(i_{d-datasheet})} \cdot \frac{f_{g-on}(r_{g-on-test})}{f_{g-on}(r_{g-on-datasheet})} \quad (16)$$

$$E_{off-tets} = E_{off-datasheet} \cdot \frac{f_{Vds-off}(V_{ds-test})}{f_{Vds-off}(V_{ds-datasheet})} \cdot \frac{f_{id-off}(i_{d-test})}{f_{id-off}(i_{d-datasheet})} \cdot \frac{f_{g-off}(r_{g-off-test})}{f_{g-off}(r_{g-off-datasheet})} \quad (17)$$

where $E_{on-datasheet}$ and $E_{off-datasheet}$ are the switch turn-on and turn-off losses in the datasheet [31]. Each parameter function (f) can be derived using curve-fitting tools. After simplification, the losses are defined based on the device current as described in (18) [31]. The total switching losses of a switch is obtained by the mean value of switching losses in a complete output ac cycle.

$$\begin{aligned} E_{on-tets} &= k_{1on} i_d^{\,2} + k_{2on} i_d + k_{2on} \\ E_{off-tets} &= k_{1off} i_d^{\,2} + k_{2off} i_d + k_{2off} \end{aligned} \quad (18)$$

The switching loss of the LF switches depends on the charge of the output capacitor (C_{oss}) of the switch. The reason is that the C_{oss} of the LF switches are charged and discharged at the switching frequency of the output voltage. In fact, the output capacitors of LF switches are in parallel with the output capacitors of HF switches. For example, during the positive half cycle when the converter is switching in sector 2, the C_{oss} of S_6 and S_7 are charged up to $V_{dc}/2$ when the vectors HP^+ (Fig. 3(b)) or HP^- (Fig. 3(c)) are applied. Therefore, these output capacitors introduce losses during charging. On the other hand, these capacitors are discharged in the OL^+ switching state (Fig. 3(d)). These capacitors are discharged through various paths depending on the system conditions, which can affect the overall converter efficiency. Fig. 8 shows a transition when the switching state of the output voltage is changed from HP^- to OL^+. During the deadtime of S_3 and S_4, if the output current has the same sign as the output voltage (Fig. 8(b)) the body diode of S_3 starts to conduct. C_{oss} of S_6 and S_7 will be discharged in the load during this transition, as this is the only path. On the other hand, if the output current has an opposite sign compared to the output voltage, the current during the deadtime closes its path through the body diode of S_4 (Fig. 8(c)). In this state (Fig. 8(c)), the voltages across C_{oss} of S_6 and S_7 are still $V_{dc}/2$. After the deadtime, when S_3 starts to conduct a path for discharging of C_{oss} of S_6 and S_7 is provided through S_2 and S_3, which this discharging can be considered as another capacitive loss.

The capacitive switching loss is calculated by the total output charge given as follows:

$$P_{cap} = \frac{1}{2} Q_{oss@V_{DS}} V_{DS} f_{sw} \quad (19)$$

where V_{DS} is the drain-source voltage and Q_{oss} is the output capacitive charge of the device at the operating voltage. As it is listed in TABLE V, Q_{oss} of Si MOSFET when the voltage across

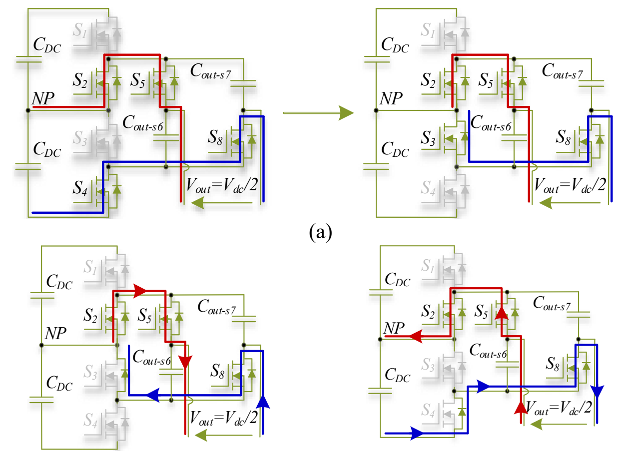


Fig. 8. The charge and discharge path of the LF output capacitors. (a) change the state from HP^- to 0^+, (b) path of current during deadtime when the load current is positive, (c) path of current during deadtime when the load current is negative.

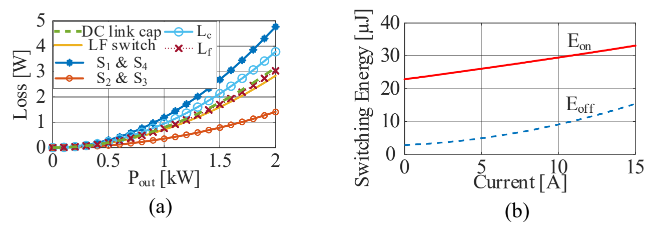


Fig. 9. The Loss simulation of the converter. (a) conduction/resistive losses, (b) switching energy losses.

it changes from 0 to $V_{dc}/2$ is 398 nC.

D. Efficiency analysis

The simulated conduction and switching energy losses at different output powers and currents are shown in Fig. 9(a) and (b), respectively. As it can be seen in Fig. 9(a), the main conduction loss is related to the top and bottom HF switches; meanwhile, the middle HF switches conduct less time. As previously stated, for n=1, only one small pair vector is used. Therefore, the HF switching loss is equal to (P_{on}+P_{off}) in this case. However, for the case n≠1, the switching loss is changed to $2(P_{on}+P_{off})$.

The main filter losses are related to copper and core losses. Since the high frequency ac copper loss is not critical for the high frequency inductors [32], in this case for L_c, a solid wire is utilized for the windings. Moreover, the current harmonic at high frequency is relatively small compared to the fundamental. The resistive losses of the filter inductors are shown in Fig. 9(a).

The core loss is associated with the changing of magnetic flux field or the high frequency current ripple in PWM filters. Therefore, the current ripple of L_c is used to calculate the core loss. Moreover, the core loss of L_f can be neglected. Among different core materials, MPP-Powder core shows an inductance independency from dc magnetization and a low core loss [32], [33]. Therefore, an MPP-Powder core is employed in the converter side inductor. Considering the DC bias performance of the core and the number of turns, the inductance behavior of the inductor can be calculated [33], and consequently, the current ripple in L_c is obtained based on (5). As a result, the magnetizing field (H), flux density (B) and core loss can be calculated through equations provided in [33], [34]. The specifications of inductors are listed in TABLE VI. At full load the core loss is equal to 0.41W; meanwhile, the conduction loss is 3.8W.

Normally, a large surge voltage appears at the output voltage of the converter due to the fast switching capability of switches and stray inductance of the package and PCB. To improve the output voltage waveform, a snubber circuit is designed and implemented [35].Therefore, the loss related to the snubber is included in the results.

V. Experimental results

The measurement setup is shown in Fig. 10. To control the converter and implement the hybrid SVM, the dSPACE's Micro-Lab Box ds1202 FPGA is utilized. The experimental results are presented in two sections: modulation and efficiency.

A. Hybrid SVM

In this experiment, parameter n which alternates the dynamic of the converter to regulate the NP voltage is under study and shown in Fig. 11. In Fig. 11 (a), when n is changed from 0.5 to 0.6, the voltages of the dc-link capacitors start to converge. For n=0.6, the required time for voltages to reach the same level is around 90ms. In Fig. 11 (b) and (c), this time is reduced to 30 and 15ms for n equals to 0.8 and 1, respectively.

As it was mentioned earlier, n affects the harmonic contents of the output voltage. Fig. 12(a) shows the FFT result of the output voltage when n is set to be 0.505. The first major harmonic is at 140kHz. In addition, the odd multiple harmonics of the switching frequency will be removed from the output voltage. By increasing n, the dynamic of the system to regulate the voltages of the dc-link capacitors increases; in return, the magnitudes of the odd multiple harmonics of the switching frequency are increased. This can be seen in Fig. 12(b) and (c), where n is increased to 0.8 and 1, respectively.

The measurement results of the output voltage, the voltage and the current across the ac load and the converter current for n = 0.505 and 1 are shown in Fig. 13. By comparing Fig. 13(c) and (f), it can be realized that the current ripple is two times larger when n=1 than n=0.505.

TABLE VI
The filter inductor parameters

inductor	core	Number of turns	Wire diameter
L_c	MPP-C055439A2	62	1.6 mm
L_f	Kool Mμ- 0077192A7	55	1.6 mm

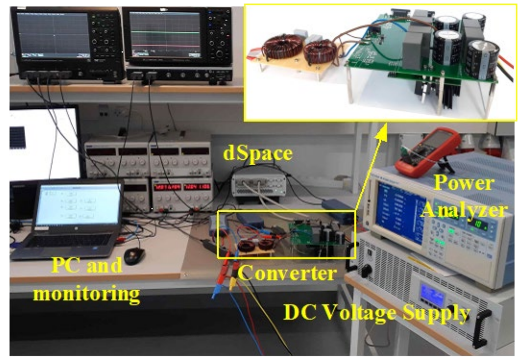
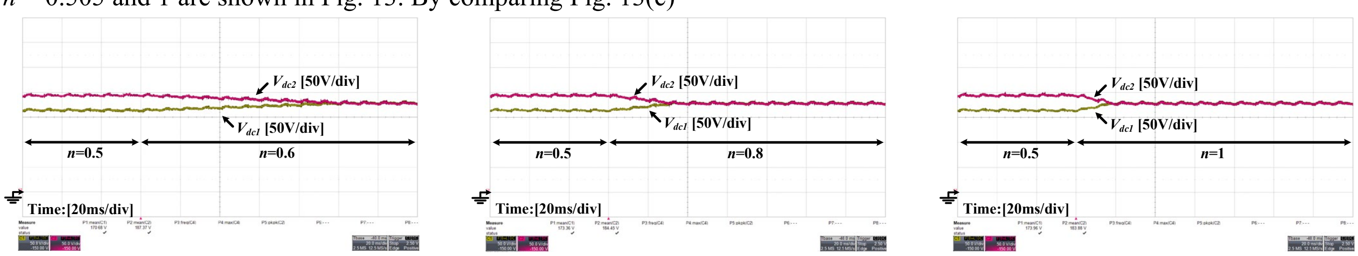


Fig. 10. The measurement setup.

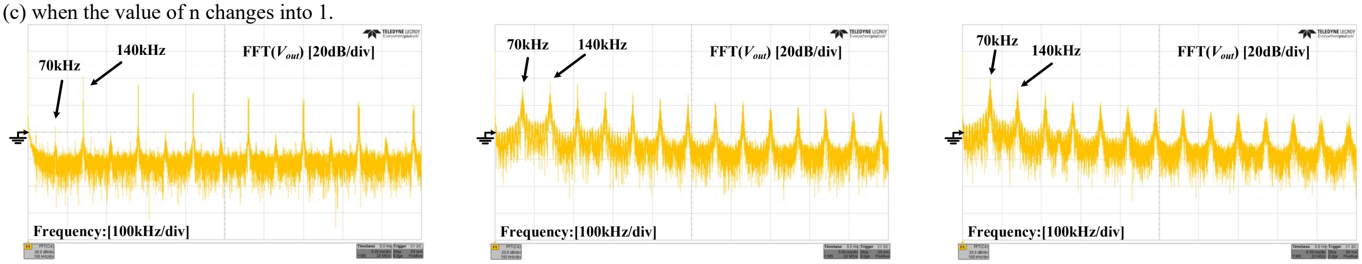
B. Efficiency

To measure the efficiency of the converter, a YOKOGAWA-WT3000 precision power analyzer for both the ac (v_f, i_f) and dc (v_{dc}, i_{dc}) sides has been utilized [see Fig. 5]. The duration between each load step is at least 10 minutes to make sure that the converter is thermally stabilized. Furthermore, the measurement's linear average mode is active, taking an average over 256 cycles. Fig. 14(a) shows the efficiency curve of the converter. Since the filter is calculated for the worst-case condition (where n = 1), the efficiency under investigation is for n = 1. However, to show the effect of smaller n on the efficiency, an additional experiment is carried out with n = 0.5 while the filter parameters has been kept constant. As expected, since the effective switching frequency of n=0.5 is double of the case with n=1, the constant power losses which is mainly the switching loss is higher in this case.



(a) (b) (c)

Fig. 11. The experimental measurements of the voltages of DC link capacitors, (a) when the value of n changes into 0.6, (b) when the value of n changes into 0.8, (c) when the value of n changes into 1.



(a) (b) (c)

Fig. 12. The FFT results of output voltage of converter for the n value of (a) 0.505, (b) 0.8, (c) 1.

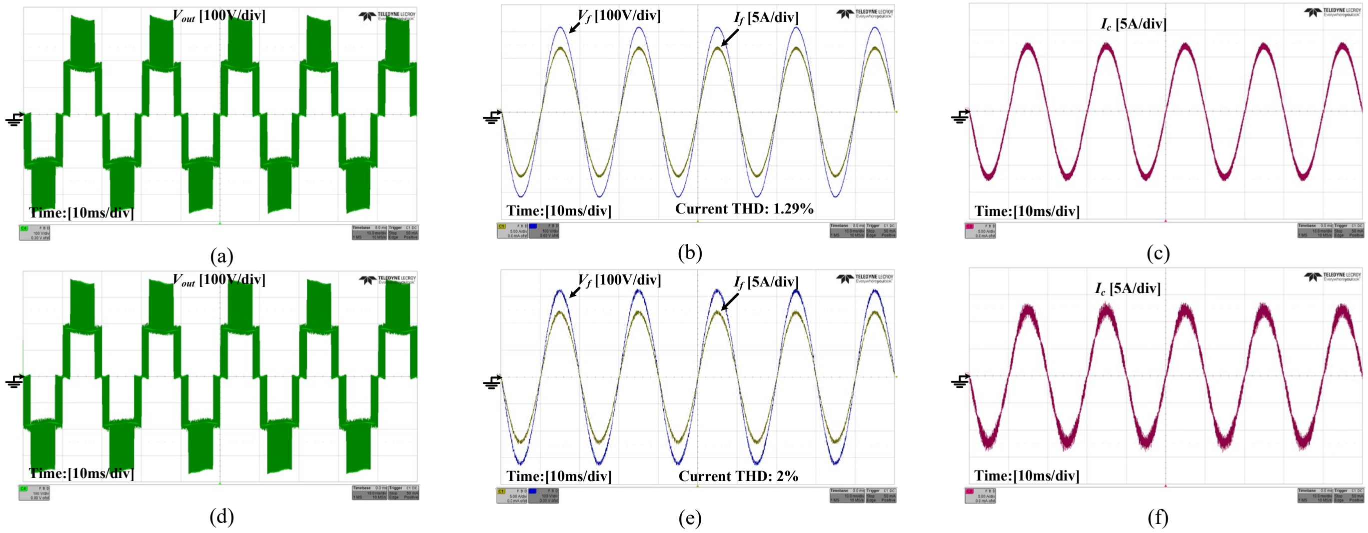


Fig. 13. The experimental measurements, (a) output voltage for n=0.505, (b) the voltage and current of AC load for n=0.505, (c) the current of the converter side inductor for n=0.505, (d) output voltage for n=1, (e) the voltage and current of AC load for n=1, (f) the current of the converter side inductor for n=1.

The loss distribution of the converter is calculated and shown in Fig. 14(b) and (c). The main difference is related to the switching loss contribution. In addition, the core loss of case n=0.5 is less than the case n=1, because the current ripple when n=0.5 is half of the case n=1. Furthermore, the THD of output current decreased from 2% for n=1 to 1.29% for n=0.5.

An efficiency comparison of single phase 5-level converters in the literature and the proposed converter is provided in TABLE VII. Compared to other converters, a flat efficiency curve is obtained in this converter.

VI. Conclusion

This paper has presented a comprehensive loss and efficiency analysis of a 2kW hybrid single-phase converter composed of SiC/Si MOSFETs. By employing the achieved redundancy of the converter topology, two different switch technologies with hybrid switching pattern are utilized to improve the efficiency of the converter. A complete efficiency analysis has been conducted through calculating the RMS current of each switch and the dc-link capacitor. To calculate the switching losses for each switch, the obtained data from the datasheet is modified based on real test conditions of the system. In order to control the NP voltage, a hybrid SVM technique with consideration of a weight coefficient was presented to change the time periods of output vectors to keep the voltages of the dc-link capacitors at the same voltage level. In addition, the effects of the weight coefficient on the efficiency of the converter has been theoretically analyzed and the efficiency is measured and compared with the analysis for the worst-case condition. It was demonstrated that weight coefficient can either improve the size or efficiency, but not both simultaneously. The experimental results of different scenarios have been presented to confirm the capability of the designed converter and proposed modified hybrid SVM to regulate the dc-link voltage. The measured efficiency for different values of the weight coefficient shows similar behavior to the analysis. The peak efficiency of 98.4% was achieved while the THD of converter current was less than 2%.

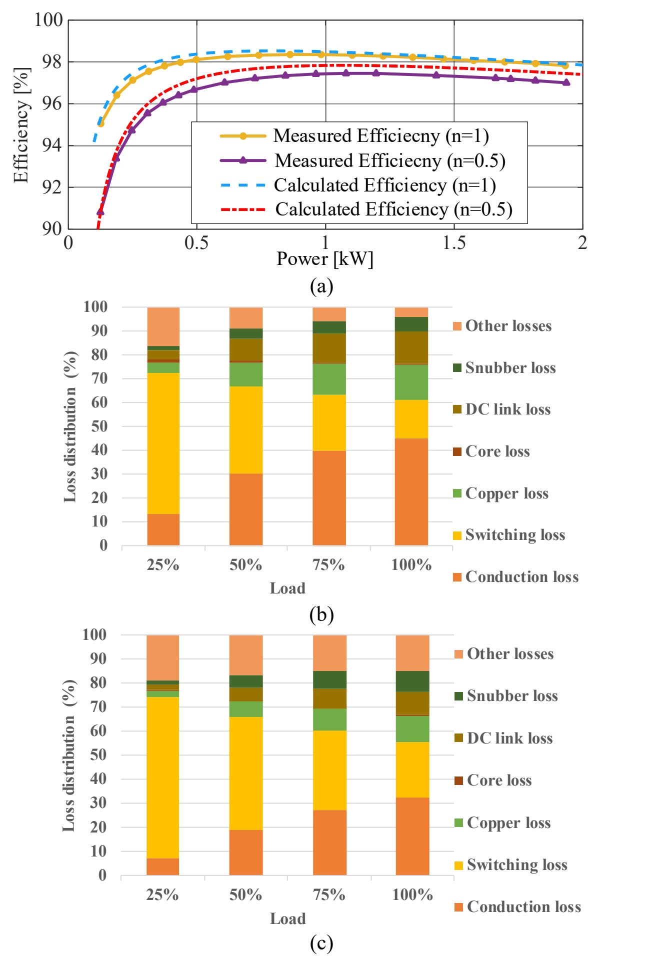


Fig. 14. The efficiency results (a) simulated and measured efficiency of the converter, (b) loss distribution for different loads when n=1, (c) loss distribution for different loads when n=0.5.

References

[1] J. I. Leon, S. Vazquez, and L. G. Franquelo, “Multilevel Converters: Control and Modulation Techniques for Their Operation and Industrial Applications,” *Proc. IEEE*, vol. 105, no. 11, pp. 2066–2081, Nov. 2017.

[2] J. Rodriguez, Jih-Sheng Lai, and Fang Zheng Peng, “Multilevel inverters: a survey of topologies, controls, and applications,” *IEEE Trans. Ind.*

TABLE VII
Efficiency comparisons of single-phase 5-level converters

Ref	Power (kW)	Switch Type	dc-link voltage (V)	Switching Frequency (kHz)	Filter Structure	Peak Efficiency	Full load Efficiency
[12]	4	SiC/Si	400	40	LC	98.1	96.5
[15]	5	IGBT	500	20	LC	98.8	96.2
[16]	0.13	n/a	200	5	LC	93.5	91.5
[17]	1.2	Si/Super-junction	200	20	LC	99	93.8
[18]	2	IGBT	200	16	LCL	97.8	97.2
[19]	0.9	Super-junction	200	25	L	98.1	98.1
[20]	1.4	IGBT	350	12	L	96.6	94
[36]	0.3	HEXFET	50	15	LC	98.6	87.8
[37]	1.2	HEXFET	100	10	L	96	93
This work	2	SiC/Si	360	70	LCL	98.4	97.8

Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.

[3] L. Zhang, K. Sun, L. Feng, H. Wu, and Y. Xing, "A family of neutral point clamped full-bridge topologies for transformerless photovoltaic grid-tied inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 730–739, 2013.

[4] S. Vazquez, P. Acuna, R. P. Aguilera, J. Pou, J. I. Leon, and L. G. Franquelo, "DC-Link Voltage-Balancing Strategy Based on Optimal Switching Sequence Model Predictive Control for Single-Phase H-NPC Converters," *IEEE Trans. Ind. Electron.*, vol. 67, no. 9, pp. 7410–7420, 2020.

[5] W. Song, X. Feng, and K. M. Smedley, "A carrier-based pwm strategy with the offset voltage injection for single-phase three-level neutral-point-clamped converters," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1083–1095, 2013.

[6] S. Wang, J. Ma, B. Liu, N. Jiao, T. Liu, and Y. Wang, "Unified SVPWM Algorithm and Optimization for Single-Phase Three-Level NPC Converters," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7702–7712, 2020.

[7] S. Vazquez *et al.*, "Model Predictive Control for Single-Phase NPC Converters Based on Optimal Switching Sequences," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7533–7541, 2016.

[8] D. Floricau, E. Floricau, and G. Gateau, "New Multilevel Converters With Coupled Inductors: Properties and Control," *IEEE Trans. Ind. Electron.*, vol. 58, no. 12, pp. 5344–5351, Dec. 2011.

[9] A. I. M. Ali, M. A. Sayed, E. E. M. Mohamed, and A. M. Azmy, "Advanced Single-Phase Nine-Level Converter for the Integration of Multiterminal DC Supplies," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 3, pp. 1949–1958, 2019.

[10] S. Luo, F. Wu, and K. Zhao, "Modified Single-Carrier Multilevel SPWM and Online Efficiency Enhancement for Single-Phase Asymmetrical NPC Grid-Connected Inverter," *IEEE Trans. Ind. Informatics*, vol. 16, no. 5, pp. 3157–3167, 2020.

[11] S. Iturriaga-Medina *et al.*, "A comparative analysis of grid-tied single-phase transformerless five-level NPC-based inverters for photovoltaic applications," *Int. Power Electron. Congr. - CIEP*, vol. 2016-Augus, pp. 323–328, 2016.

[12] L. Zhang, Z. Zheng, and C. Li, "A Si / SiC Hybrid Five-Level Active NPC Inverter," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 4835–4846, 2020.

[13] A. Kahwa, H. Obara, and Y. Fujimoto, "Design of 5-level reduced switches count H-bridge multilevel inverter," in *2018 IEEE 15th International Workshop on Advanced Motion Control (AMC)*, 2018, pp. 41–46.

[14] R. González, J. López, P. Sanchis, and L. Marroyo, "Transformerless inverter for single-phase photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 693–697, 2007.

[15] J. A. F. Neto, R. P. T. Bascope, C. M. Cruz, R. G. A. Cacau, and G. V. T. Bascope, "Comparative evaluation of three single-phase NPC inverters," *2012 10th IEEE/IAS Int. Conf. Ind. Appl. INDUSCON 2012*, no. 1, 2012.

[16] Y. Hu, Y. Xie, D. Fu, and L. Cheng, "A New Single-Phase Π-Type 5-Level Inverter Using 3-Terminal Switch-Network," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7165–7174, Nov. 2016.

[17] B. Shaffer, H. A. Hassan, M. J. Scott, S. U. Hasan, G. E. Town, and Y. Siwakoti, "A common-ground single-phase five-level transformerless boost inverter for photovoltaic applications," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, vol. 2018-March, pp. 368–374, 2018.

[18] G. E. Valderrama, G. V Guzman, E. I. Pool-Mazún, P. R. Martinez-Rodriguez, M. J. Lopez-Sanchez, and J. M. S. Zuñiga, "A Single-Phase Asymmetrical T-Type Five-Level Transformerless PV Inverter," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 1, pp. 140–150, Mar. 2018.

[19] N. Vosoughi, S. H. Hosseini, and M. Sabahi, "A New Transformer-Less Five-Level Grid-Tied Inverter for Photovoltaic Applications," *IEEE Trans. Energy Convers.*, vol. 35, no. 1, pp. 106–118, 2020.

[20] F. B. Grigoletto, "Five-Level Transformerless Inverter for Single-Phase Solar Photovoltaic Applications," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 4, pp. 3411–3422, 2020.

[21] G. W. Chang, H. W. Lin, and S. K. Chen, "Modeling characteristics of harmonic currents generated by high-speed railway traction drive converters," *IEEE Trans. Power Deliv.*, vol. 19, no. 2, pp. 766–773, 2004.

[22] S. Wang, W. Song, J. Zhao, and X. Feng, "Hybrid single-carrier-based pulse width modulation scheme for single-phase three-level neutral-point-clamped grid-side converters in electric railway traction," *IET Power Electron.*, vol. 9, no. 13, pp. 2500–2509, 2016.

[23] J. Salaet, A. Gilabert, J. Bordonau, S. Alepuz, A. Cano, and L. M. Gimeno, "Nonlinear control of neutral point in three-level single-phase converter by means of switching redundant states," *Electron. Lett.*, vol. 42, no. 5, pp. 304–306, Mar. 2006.

[24] Z. Zhang, Y. X. Xie, W. P. Huang, J. Y. Le, and L. Chen, "A new SVPWM method for single-phase three-level NPC inverter and the control method of neutral point voltage balance," *Proc. - 12th Int. Conf. Electr. Mach. Syst. ICEMS 2009*, pp. 9–12, 2009.

[25] T. B. Soeiro, K.-B. Park, and F. Canales, "High voltage photovoltaic system implementing Si/SiC-based active neutral-point-clamped converter," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, 2017, pp. 1220–1225.

[26] M. Farhadi Kangarlu, E. Babaei, and F. Blaabjerg, "an Lcl-Filtered Single-Phase Multilevel Inverter for Grid Integration of Pv Systems," *J. Oper. Autom. Power Eng.*, vol. 4, no. 1, pp. 54–65, 2016.

[27] E. Babaei, M. F. Kangarlu, and M. Sabahi, "Extended multilevel converters: An attempt to reduce the number of independent DC voltage sources in cascaded multilevel converters," *IET Power Electron.*, vol. 7, no. 1, pp. 157–166, 2014.

[28] A. Kouchaki and M. Nymand, "Analytical Design of Passive LCL Filter for Three-Phase Two-Level Power Factor Correction Rectifier," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3012–3022, 2018.

[29] A. K. Sadigh, V. Dargahi, and K. A. Corzine, "Analytical Determination of Conduction and Switching Power Losses in Flying-Capacitor-Based Active Neutral-Point-Clamped Multilevel Converter," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5473–5494, 2016.

[30] A. Anthon, Z. Zhang, M. A. E. Andersen, D. G. Holmes, B. McGrath, and C. A. Teixeira, "The benefits of SiC mosfets in a T-type inverter for grid-tie applications," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2808–2821, 2017.

[31] Q. X. Guan *et al.*, "An Extremely High Efficient Three-Level Active Neutral-Point-Clamped Converter Comprising SiC and Si Hybrid Power Stages," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8341–8352, 2018.

[32] A. Kouchaki and M. Nymand, "High efficiency three-phase power factor correction rectifier using SiC switches," *2017 19th Eur. Conf. Power Electron. Appl. EPE 2017 ECCE Eur.*, vol. 2017-Janua, 2017.

[33] MAGNETICS, "POWDER CORES," 2020.

[34] J. Wang, N. Rasekh, X. Yuan, and K. J. Dagan, "An Analytical Method for Fast Calculation of Inductor Operating Space for High-Frequency Core Loss Estimation in Two-Level and Three-Level PWM Converters,"

IEEE Trans. Ind. Appl., vol. 57, no. 1, pp. 650–663, 2021.
[35] ROHM Semiconductor, “SiC MOSFET Snubber circuit design methods.”
[36] L. He and C. Cheng, “A Flying-Capacitor-Clamped Five-Level Inverter Based on Bridge Modular Switched-Capacitor Topology,” *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7814–7822, 2016.
[37] M.-K. Nguyen and T.-T. Tran, “Quasi Cascaded H-Bridge Five-Level Boost Inverter,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8525–8533, 2017.

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His main research interests are compact and highly efficient switch-mode power supplies, magnetic design, and high-power converters for battery chargers and renewable energy.