



Design and FPGA-in-loop based validation of predictive hierarchical control for islanded AC microgrid

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ABSTRACT

This paper proposes a decentralized control approach for the flexible operation of an autonomous AC microgrid (MG). AC MG typically consists of two or more voltage source inverters (VSI), capable of simultaneously regulating the voltage at the point of common coupling (PCC) and meeting the local power demand. The classical linear control techniques attain these functions. However, they have many limitations, such as slow transient response, high sensitivity to the parameter variations, and inability to handle the system nonlinearities. This paper aims to address these issues by presenting an improved finite control set model predictive control (FCS-MPC) approach for inverter-based distributed generation (DG). The proposed scheme tracks the voltage trajectory using cost function (CF) over two-step prediction horizons. The proposed control method is employed for the AC MG having two parallel DGs. Droop control is responsible for the power-sharing between the parallel DGs regardless of impedance mismatch at the distribution level of AC MG. The decentralized secondary control is developed to eliminate the deviation in the voltage and frequency caused due to overlooking the primary control. The proposed control scheme has been validated through extensive simulations and real-time controller hardware in the loop tests using an FPGA ZYBO Z7 board. Moreover, the proposed methodology depicts the enhanced transient response, less computational burden than the classic MPC, and shows robustness to parametric uncertainties in terms of THD than hierarchical linear control. The simulations and experimental results visually represent research outcomes, exhibiting the THD of 0.98 % for different dynamic loads, which is within the limit of IEEE and IEC standards. Furthermore, the proposed controller's mathematical stability is further supported by analysis based on the Lyapunov stability theory.

1. Introduction

Due to climate change and global warming, various countries in the world adopted the Paris Agreement to reduce the emission of greenhouse gases and also limit global warming below the 2 °C [1]. Power generation through fossil fuels such as oil, coal, and natural gas is one of the primary causes of greenhouse gases emission. The world is looking for alternative ways of energy generation, which must be clean, reliable, and carbon-free. Therefore, power generation through renewable energy sources has got the world's attention. However, renewable energy resources (RES) are intermittent and produce energy in both AC and DC. Consequently, the concept of distributed generation (DG) is introduced in literature by the research community to integrate RES in conventional power systems and meet the load demand locally [2].

The DGs are connected to the grid through a power electronic interface (PEI). PEIs are responsible for regulating the voltage, current, and power. The high penetration and integration of RES in the power system originate high risks to the power system's stability and reliability.

The microgrid (MG) concept is presented to mitigate the problems as mentioned [3,4]. MG is a small distribution power system with a cluster of loads, generation units, and energy storage systems, and it effectively controls each unit [5]. The MG can operate in two modes, i.e., grid-connected and islanded modes. In grid-connected mode, MG has the ability to import and export the power with the utility grid as per grid codes such as EN 50549-1 or EN 50549-2 [6]. In islanded mode, MG is disconnected from the main grid due to regular maintenance, low-quality power generation, or occurred faults. The autonomous MG is also developed for areas far from the power network, such as rural areas. Islanded MG is used in various applications such as avionic [7], marine [8] and automotive [9]. Sometimes, it is economical to distribute the high power among the several DGs with lower current ratings. This mechanism also helps to maximize the system's efficiency. The islanded MG generates power to meet the demand locally and also regulates the voltage at the point of common coupling. However, an energy management system is required to run and optimize the operation of an islanded MG.

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Nomenclature

ANN	Artificial Neural Network
CF	Cost Function
CI	Constant Current
CZ	Constant Impedance
CP	Constant Power
DSO	Distribution System Operator
DG	Distributed Generation
DER	Distributed Energy Resources
MG	Microgrid
MPC	Model Predictive Control
MPVC	Model Predictive Voltage Control
PEI	Power Electronic Interface
PC	Power Converter
PI	Proportional Integral
PR	Proportional Resonant
PCC	Point of Common Coupling
SOGI-PLL	Second Order Generalized Integrator Phase Locked Loop
TSO	Transmission System Operator
THD	Total Harmonic Distortion
VSI	Voltage Source Inverter
VSC	Voltage Source Converter

The MG control approaches are categorized as distributed, decentralized, and centralized in literature [10]. Distributed and centralized control techniques require a communication network. The implementation of centralized techniques reduces reliability and increases system complexity. However, the decentralized approach uses local measurements and does not require any communication infrastructure [11].

The hierarchical control of MG is vastly proposed in the literature and it is considered to be the best possible solution to regulate the MG operation. Fig. 1 explains the hierarchical control graphically for easy understanding. MG hierarchical control consists of three different levels, i.e., primary, secondary, and tertiary levels [12,13].

- **Primary control:** It is further divided into inner control and outer droop control loops. The inner control loop regulates the output current and voltage of DERs. The outer droop control is responsible for accurate power-sharing among the DGs and also mitigates the circulating current.
- **Secondary control:** This control level is responsible for mitigating the MG's voltage and frequency deviation. The response of this level is slower than the primary controller.
- **Tertiary Control:** This control level is at the highest level of the MG hierarchy, and its response is slower than the secondary control loop. It is responsible for scheduling and optimizing power generation references for DGs and the techno-economic operation of MG and remains in contact with DSO and TSO.

As aforementioned that tertiary control focuses on economic dispatch and operation scheduling. It is also characterized as coordination between multiple MG, which are interconnected. In [14] tertiary control is implemented to adjust the DG compensating efforts with respect to unbalanced voltage limits of DGs and load buses. Optimal power flow-based tertiary control using MPC is proposed in [15]. In [16], authors proposed a centralized IOT-based tertiary control solution for multi-microgrids.

Many studies are proposed in the literature incorporating primary and secondary control levels and implementing the amalgam of linear and nonlinear controllers. Hierarchical control for grid supporting inverter in AC MG is investigated in [17]. PR based inner and PI based

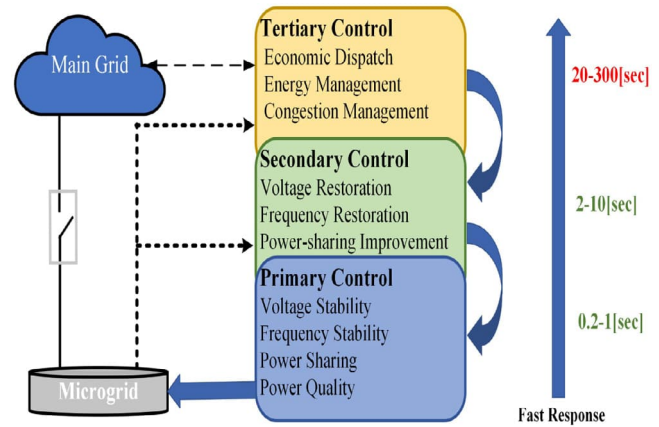


Fig. 1. Control layers typically utilized for hierarchical control of MGs.

secondary loops are proposed in [18] for the islanded AC microgrid. However, multiple resonant controllers are connected in parallel to cope with the fifth and seventh harmonics, which makes the system complex and takes the system towards instability. In [19], the authors proposed the hierarchical control for MG. The PI based linear controller is implemented in the microgrid's (primary and secondary) control levels. However, linear-based controllers cannot track the sinusoidal wave with zero steady state error and poor disturbance rejection capability and cannot handle the power systems' nonlinearity. Flexible secondary control for three VSIs operated in parallel is proposed in [20]. The authors also proposed a new algorithm to optimally tune the various gain of PR controllers. MPC based primary and secondary control is proposed in [21,22]. The predictive voltage hierarchical control for islanded MC with limited communications is studied in [23]. However, implementing predictive control at the secondary level is unsuitable due to the computational burden. Implementing MPC at the secondary level increases the system complexity and decreases the system response due to computational burden. Table 1 summarizes some of the recent studies on the hierarchical control of MG based on different control typologies.

The main task of primary control is to regulate the voltage and also achieve accurate power sharing among the DGs. Different types of linear and nonlinear control techniques have been proposed and investigated in the literature [29]. Linear controllers are limited in their ability to handle the nonlinearities and parameter variations of power systems, as well as other practical issues such as the need for tuning parameters and potential stability problems [20]. Nonlinear controllers perform better than linear controllers but have limitations, such as complex mathematical modeling [30], variable switching frequency [31], and high computational burden [32]. In [33], the author proposed sliding mode control for voltage regulation of a standalone DC/AC converter. Nevertheless, the complex mathematical modeling and chattering (an undesirable phenomenon) reduce the system's performance. MPC based hierarchical control for AC MG is proposed in [34] but the authors did not test the proposed under different dynamic loads and THD (%) is more than the proposed scheme.

The artificial neural network (ANN) aided MPC based voltage regulation technique is proposed in [35,36]. The authors use the MPC as the parent system to train the ANN. The performance of ANN is better than MPC in terms of total harmonic distortion (THD) and computational burden. However, the control technique needs to be more mature. The PID controller and its combinations are matured and vastly implemented by the power electronics industry. However, the nonlinear or advanced control approaches need complex mathematical modeling, and their implementation requires high-speed digital platforms. Table 2 summarized the pros and cons of different advanced control techniques.

Table 1
Comparison of hierarchical control approaches.

References	Control levels			Secondary control scheme	Applications
	Primary	Secondary	Tertiary		
[17]	H/SMC	Agent-based	–	Distributed	Grid-supporting converter
[18]	PR	PI	–	Centralized	VSI
[19,20]	PI	PI	–	Centralized	MG
[21]	MPC	MPC	–	Decentralized	MG
[24]	PI	PI	–	Centralized	MG
[16]	–	–	IOT based	Centralized	MG
[23]	Non-linear control (Lyapunov function)	Event predicted control	–	Centralized	MG
Proposed	MPC	PI	–	Decentralized	MG

Table 2
Comparison of the different linear and nonlinear control techniques.

	Linear control (Generalized)	Slide mode control	Artificial neural network	Model predictive control
Theoretical background	Mature	Mature	Weak	Mature
Computational Complexity	Low	Medium	Low	High
Handling system constraints	Incapable	No	Yes	Yes
Parameter sensitivity	No	Robust	Data dependent	Tunable
Intuitive Design	Average	Medium	Not-studied	Yes
Stability Analysis Tool	Strong	Strong	No	Initial results
Handling non-linearities	No	Yes	Yes	Yes
Frame of Reference	DQ	ALL	ALL	ALL
Implementation	[19,20]	[25]	[26,27]	[28]

This study aims to develop and implement the decentralized hierarchical control technique for attaining enhanced transient stability and accurate power sharing among the DGs under different dynamics loads in islanded AC MG. Fig. 6 elucidates the implemented hybrid MPC-based hierarchical control for DG. The key contributions in this study are as follows:

1. The finite control set model predictive voltage control is introduced at the primary layer to regulate the voltage of the DG and droop control is also implemented to attain accurate power-sharing among the DGs under complex load conditions. MPC uses DER's discrete time domain model to anticipate the future voltage states for each possible switching combination in every sampling time. This technique determines the error using the pre-defined cost function and produces optimal control action for the coming instant based on the error minimization. In order to reduce the switching loss, the switching frequency reduction technique is implemented based on [37].
2. Lyapunov stability studies are carried out to validate the stability of the proposed controller. According to the authors' best knowledge, this analysis has not been previously carried out for 2-level DC/AC three-phase inverters.
3. At the secondary control level, the PI controller based frequency and voltage regulation loop are employed to annihilate the voltage and the frequency deviation overlooked by the primary control in AC MG. The proposed technique uses local measurements to regulate the voltage and frequency of MG.
4. The impact of different dynamics loads, such as commercial, residential, and constant power, on the proposed controller is also studied and evaluated.

Additionally, to validate the system performance in real time, the controller hardware in the loop (CHIL) testing is carried out using the FPGA ZYBO Z7 board. The proposed controller runs on the FPGA board while AC MG is simulated in MATLAB/Simulink. The JTAG

cable is used for two way communication. Finally, we also provide an [GitHub¹](https://github.com/HS-Khan/-PREDICTIVECONTROLUsingFPGAZYNQ7020) open repository of the dataset and simulation files and ZYBO Z7 (ZYNQ-7020) board definition files (to integrate the board into the MATLAB FPGA Manager for HIL validation) to the community for further research activities.

The rest of the paper is organized as follows: Section 2 explains the structure of MG. Section 2.1 describes the discrete modeling of DER and MPC and the switching reduction method is written in Section 2.2. The Lyapunov function MPC stability for DC/AC converter is derived in Section 2.3. Section 2.4 discusses the virtual impedance loop while the droop control and its implementation are expressed in Section 2.5. PI-based secondary control and its stability analysis are studied in Section 3. Dynamics loads and their mathematical modeling is explained in Section 4. Section 5 discusses the simulation studies. In contrast, HIL testing of the proposed control scheme is discussed in Section 5.1 while parametric uncertainty tests are presented in Section 5.2. Finally, the conclusion is presented in Section 6.

2. Microgrid

Fig. 2 illustrates the common configuration of a microgrid, which contains multiple DGs, loads, the energy storage system (ESS), transmission lines, and their effective control. MG is connected to the utility grid through a circuit breaker or static transfer switch. DGs are connected to an AC bus through a feeder. MG has the ability to work in grid connected or islanded mode. In this study, only islanded mode operation of MG is studied. Fig. 1 expressed the hierarchical control layers of MG and their roles. Since tertiary control has no role in islanded operation mode, it is not taken into account in this study. Droop control and virtual impedance loop are also discussed in this section.

¹ <https://github.com/HS-Khan/-PREDICTIVECONTROLUsingFPGAZYNQ7020>

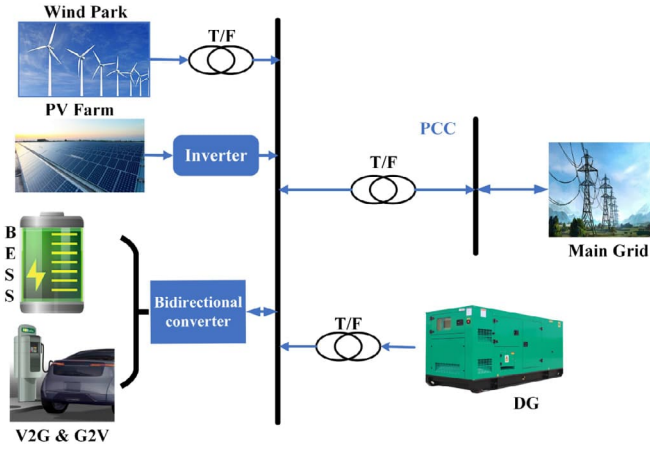


Fig. 2. Possible configuration of an islanded AC MG.

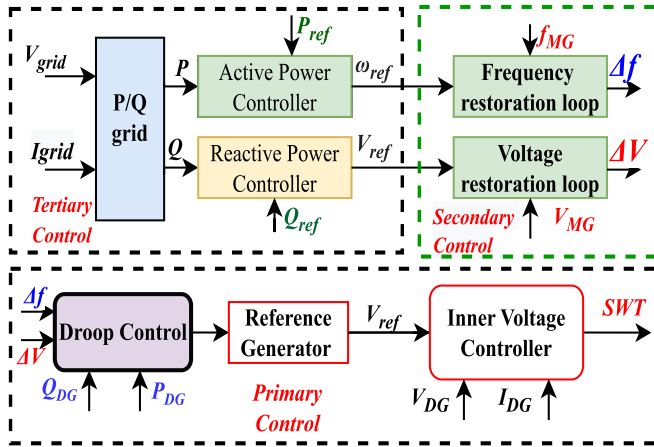


Fig. 3. Classical hierarchical control configuration of islanded AC MG.

2.1. MPC based primary control

This section discusses the discrete time modeling of VSI, the MPC's basic working principle, and its cost function definition. Fig. 3 demonstrates the classical hierarchical control implemented in literature for readers' better understanding. This study uses the Clarke transformation [38,39] to formulate the primary control in the $\alpha\beta$ reference frame. However, the performance of MPC in all frames of reference is evaluated to be the same [40].

The inner control of VSI is based on FCSMPC because it has better performance under transient conditions, the ability to handle the non-linearity, good disturbance rejection capacity, and improved reference tracking capability [22]. The power converter's discrete-time model and filter are employed to anticipate the future response of DG for probable eight (2^3) switching states. Among these, six states are stated as active states, while two states with zero output are known as zero states as expressed in Eq. (1). The control approach based on MPC theory chooses the switching state, which has the least value of CF among them and is implemented for the next sampling time. Fig. 6 presents the two level three phase voltage source inverter with an LC filter to mitigate the switching harmonics. Each leg of VSC has two switches; they can be in on or off state and represented as 1 and 0, respectively. The output voltage of the VSI depends upon the switching

states (000, 100, 110, 010, 011, 001, 101, & 111). At every switching action, VSI has a different output value and is expressed as follows:

$$V_0 = \begin{cases} \frac{2}{3} V_{dc} e^{j(i-1)\frac{\pi}{3}} & (i = 1, 2, \dots, 6) \\ 0 & (i = 0, 7) \end{cases} \quad (1)$$

The mathematical model of the VSI and its filter can be determined by using Kirchhoff voltage and current law. Eqs. (2) and (3) express the dynamic behavior of the capacitor and inductor, respectively. I_{fabc} is the inductor current through inductor L_f while V_{0abc} is the voltage across capacitor C_f , and i_{0abc} is the output current. V_i is the output of the converter. The equations are as follows:

$$\frac{1}{C_f} \frac{dV_{0abc}(t)}{dt} = i_f(t) - i_{0abc}(t). \quad (2)$$

$$V_i = i_f(t)R_f + L_f(t) \frac{di_f(t)}{dt} + V_{0abc}(t) \quad (3)$$

The state space model of the system is determined by combining Eqs. (2) and (3) and written as:

$$\frac{d(y)}{dt} = Ax + By \quad (4)$$

In Eq. (5), the x matrix represents the system's state variables, and the y matrix explains the output variables of the system.

$$x = \begin{bmatrix} V_{0abc} \\ i_f \end{bmatrix}, y = \begin{bmatrix} V_i \\ i_{0abc} \end{bmatrix} \quad (5)$$

$$A = \begin{bmatrix} 0 & \frac{1}{C_f} \\ -\frac{1}{L_f} & -\frac{R_f}{L_f} \end{bmatrix}, B = \begin{bmatrix} 0 & -\frac{1}{C_f} \\ \frac{1}{L_f} & 0 \end{bmatrix} \quad (6)$$

By solving Eq. (4) using Euler's technique, the discrete time model of the system can be expressed as:

$$\begin{bmatrix} V_{0abc}(t_k + 1) \\ i_f(t_k + 1) \end{bmatrix} = A_r \begin{bmatrix} V_{0abc}(t) \\ i_f(t) \end{bmatrix} + B_r \begin{bmatrix} V_i(t) \\ i_{0abc}(t) \end{bmatrix} \quad (7)$$

$$A_r = e^{AT_s} \approx 1 + AT_s, \quad B_r = \frac{B}{A} (A_r - I) \quad (8)$$

where "t" represents the present instant, while $t_k + 1$ is the future sampling instant. Eq. (7) is used to pre-calculate the capacitor voltage for all feasible voltage vectors in the coming instant.

The definition of CF is essential in the design of MPC. CF is used to calculate the lowest error while handling multiple objectives. It is the error between the predefined reference and actual values. The general CF equation is presented in Eq. (9).

$$g_{\text{Gen}} = \sum_{i=k}^{t_k+N-1} \|v_{fe}(i)\|_2^2 + h_{\text{lim}}(i) + \lambda_u sw^2(i) \quad (9)$$

where v_{fe} is the anticipated tracking error and primary objective while secondary objectives are $h_{\text{lim}}(i)$ is the current limitation, $sw^2(i)$ defines the reduction of switching frequency and is regulated by weighting factor λ . The CF defined in this study is only based on the primary objective (Voltage) and is expressed as follows:

$$G_{\text{primary}} = (V_{0\alpha}^* - V_{0\alpha}^{(t_k+1)})^2 + (V_{0\beta}^* - V_{0\beta}^{(t_k+1)})^2 \quad (10)$$

where $V_{0\alpha\beta}^*$ represents the reference voltage for DG in the $\alpha\beta$ reference frame, and $V_{0\alpha\beta}^{(t_k+1)}$ is determined using Eq. (7). The reference voltage is provided by the droop control. The DC-link capacitor voltage is taken as constant throughout the modeling. The working process of the MPVC is illustrated in the flowchart as shown in Fig. 4. After the controller's initialization, measured inputs are taken by the controller to predict the one step ahead voltage and current using Eq. (7). Eq. (10) is used to determine the value of the CF for each possible switching state of the converter. Among all possible switching states, the switching state, which has minimal error value, is applied to the converter for the next switching instant.

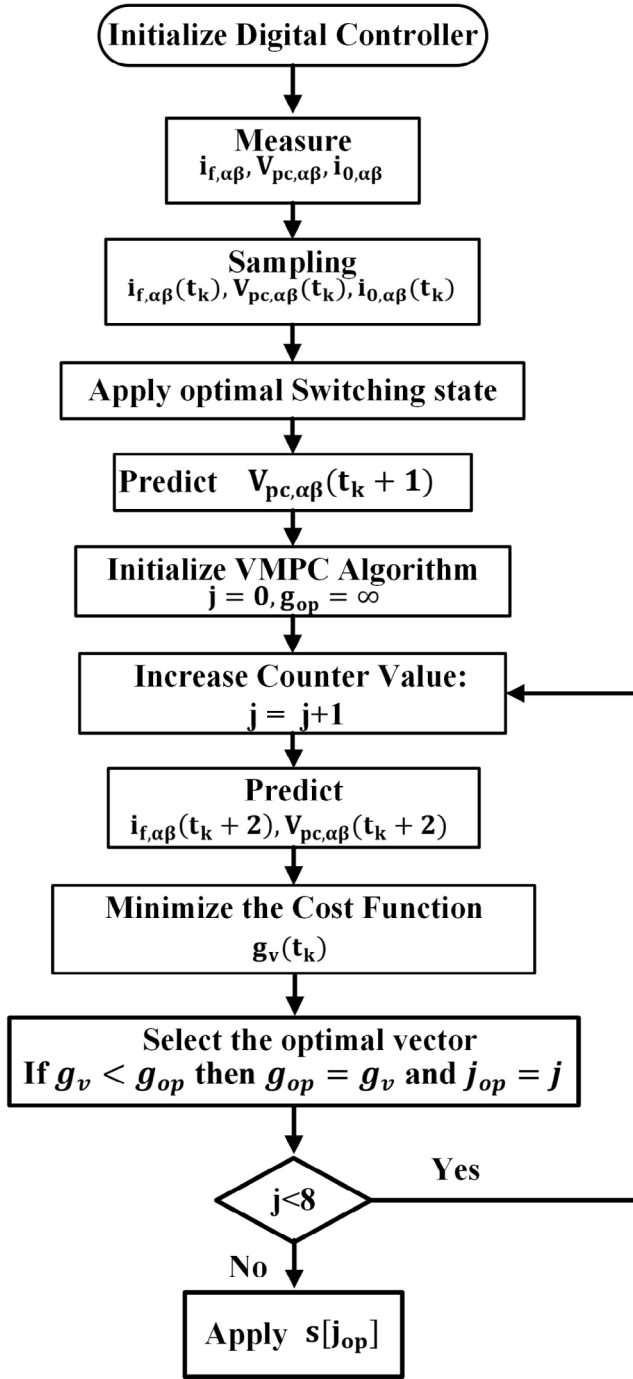


Fig. 4. Flow chart of the proposed predictive controller.

2.2. Two steps ahead switching frequency reduction scheme

The power converters' switching frequency has a major effect on systems' losses. If the switching frequency is high, more loss and more stress on the converter switches will consequently occur, reducing the converter's life and decreasing the system's efficiency. Classical MPC has higher switching losses due to high switching frequency. In order to cope with this issue, a two step ahead reduction approach is implemented in this study. For two level VSI, the converter has

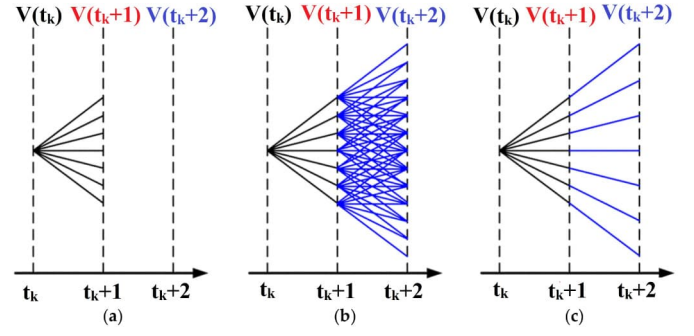


Fig. 5. Demonstration of prediction approach. (a) $N = 1$, (b) $N = 2$, and Different voltage vectors are used every sampling time. (c) $N = 2$, but the same vector is considered for two consecutive sampling times.

eight possible switching states (six active and two zero vector states) in one sampling instant, as shown in Fig. 5a. The switching state fulfills the CF criteria and is applied to the converter for the next sampling instant. In the two steps ahead classical approach, the total possible sequences are 49. So, The algorithm has to run the loop for 49 times, which increases the computation burden and also enhances the MPC performance, as demonstrated Fig. 5b. In this study, the two step prediction is accomplished by taking only eight vectors into account, as illustrated in Fig. 5c. This technique showed similar performance but had a lower switching frequency and computational burden hence using fewer hardware resources and improving the voltage quality in the form of lower THD. The predicted voltage for instant $(t_k + 2)$ is determined by Eq. (7).

2.3. MPC stability analysis

In the case of a linear theory based controller, the power electronic system is considered a linear system. In contrast, the nonlinear controller uses a power electronic system in a discrete time. So, the analysis methods based on eigenvector, bode plot, etc., are not ideal for finding the MPC stability. The Lyapunov stability criteria are widely used for the stability analysis of nonlinear controllers. There is no proper mathematical method to prove MPC stability, but many studies incorporate the Lyapunov stability to establish MPC stability. In [41], a statistical model checking approach is proposed to validate the MPC stability in the PC domain. The Lyapunov function based MPC is proposed for a four leg inverter in [42]. In [43], the authors studied the stability of MPC based on Lyapunov theory for AC/DC converters in battery applications. According to the author's best knowledge, the Lyapunov-based stability for a two level three phase DC/AC converter has not been derived before. In [44,45], multiple simulations are carried out with different system parameters to validate the response of the power converter under model uncertainties and parametric variations. The results of simulations are also verified by experiments and compared with the classical PI benchmark model. It is observed from the results that the control performance deteriorates for underestimated inductance and has no effect on the overestimated inductance. The described cases demonstrate a good steady state and transient response. The downside of this type of study is that the experiments are very time consuming. Table 3 illustrates the overview of literature work done in the domain of performance and stability of FCS-MPC.

The discrete Lyapunov function is expressed as:

$$L(k) = \frac{1}{2} [V_{err}]^T [V_{err}] \quad (11)$$

Table 3

Summary of the state-of-the-art stability and validation of FCS-MPC.

Application	Technique	Pros	Cons	Stability study	Performance validation
DC-DC converter [46] Multicell converter [47]	Lyapunov stability theory	Lyapunov stability theory (verification)	Complex cost function design	Yes	Yes
Multi-Modular converter (MMC) [44] 4-leg VSC [45]	Multi simulations, Parameter changing	Easy, fast, simple CF design	Close loop stability not defined, not validated	No	Yes
Active front end rectifier [48]	Lyapunov stability criteria	Lyapunov stability theory (verification)	Complex CF design, Not a classical MPC	Yes	No
2L-VSC [49]	Lyapunov stability theory	Easy, fast, simple CF design	Close loop stability not defined, not validated	Yes	No
VSC [41]	Benchmarking, Multiple experiments	Design for industrial engineers	Time consuming, Benchmarking	Yes	Yes
Proposed	Lyapunov stability theory	Verified	based on mathematical modeling	Yes	Yes

where V_{err} is the voltage tracking error. The change in the Lyapunov function is as follows:

$$\Delta L(k) = L(V_{err}[t+1]) - L(V_{err}[t]) \quad (12)$$

The system is asymptotically stable if the input $V_{err}(t) \in A$ and also satisfies Eq. (13) or Eq. (14). Basically, Eq. (14) is the further elaboration of Eq. (13).

$$\|L(V_{err}[t+1]) - L(V_{err}[t])\|_s \leq L_1 \|V_{err}[t+1] - V_{err}[t]\| \quad (13)$$

$$\|L(V_{err}[t+1]) - L(V_{err}[t])\| \geq L_2 \|V_{err}[t+1] - V_{err}[t]\| \quad (14)$$

$$\Delta V(t) < -L_3 \|V_{err}[t]\|^s + L_4 \quad (15)$$

where $L_1 - L_4$ must be positive values and $s \geq 1$. A is a positively invariant set of natural numbers. Now, define the inverter output voltage at $t+1$ sampling instant and express it as:

$$\vec{V}_i[t+1] = \vec{V}_i[t] + \Delta[t+1] \quad (16)$$

$\vec{V}_i[t+1]$ is the continuous voltage input vector, and $\Delta[t+1]$ represents quantization error and satisfies the condition given in Eq. (16). Where is the quantization error upper limit and is greater than 0:

$$|\Delta(t+1)| \leq \delta_1 \quad (17)$$

The change in the Lyapunov function for converter output voltage is:

$$\begin{aligned} \Delta V(t) = & \frac{1}{2} \left(\frac{1}{k_3} V_i(t+1) - \frac{k_1}{k_3} i_{0abc}(t+1) - \frac{k_2}{k_3} V_{0abc}(t+1) \right. \\ & - \frac{k_4}{k_3} i_f - V_0^*(t+1) \left. \right)^T \cdot \left(\frac{1}{k_3} V_i(t+1) - \frac{k_1}{k_3} i_{0abc}(t+1) \right. \\ & - \frac{k_2}{k_3} V_{0abc}(t+1) - \frac{k_4}{k_3} i_f - V_0^*(t+1) \left. \right) \\ & - \frac{1}{2} [V_{err}(t)]^T [V_{err}(t)] \end{aligned} \quad (18)$$

where

$$\begin{aligned} k_1 = \frac{L_f}{T_s}, k_2 = \left(1 - \frac{L_f}{T_s}\right), K_3 = \frac{L_f C_f}{T_s^2}, \\ k_4 = \frac{R_s T_s - L_f}{T_s} \end{aligned} \quad (19)$$

Now rewrite Eq. (18) as per Eq. (16) by converting the load voltage, current, and inverters voltage vector into vector and quantization error.

Here, $\delta_1(t+1), \delta_2(t+1), \delta_3(t+1)$ are the quantization errors.

$$\begin{aligned} \Delta V(t) = & \frac{1}{2} \left(\frac{1}{k_3} V_i(t+1) + \frac{1}{k_3} \delta_1(t+1) - \frac{k_1}{k_3} i_{0abc}(t+1) \right. \\ & - \frac{k_1}{k_3} \delta_2(t+1) - \frac{k_2}{k_3} V_{0abc}(t+1) - \frac{k_2}{k_3} \delta_3(t+1) - \frac{k_4}{k_3} i_f \\ & - V_0^*(t+1) \left. \right)^T \cdot \left(\frac{1}{k_3} V_i(t+1) + \frac{1}{k_3} \delta_1(t+1) \right. \\ & - \frac{k_1}{k_3} i_{0abc}(t+1) - \frac{k_1}{k_3} \delta_2(t+1) - \frac{k_2}{k_3} V_{0abc}(t+1) \\ & - \frac{k_2}{k_3} \delta_3(t+1) - \frac{k_4}{k_3} i_f - V_0^*(t+1) \left. \right) - \frac{1}{2} [V_{err}(t)]^T [V_{err}(t)] \end{aligned} \quad (20)$$

The VSI voltage vector, load current, and voltage are finite sets and bounded. The change of defined control error in Eq. (15), can be written as:

$$\begin{aligned} \Delta V(t) \leq & -\frac{1}{2} [V_{err}(t)]^T [V_{err}(t)] \\ & + \frac{1}{2} \left(\frac{1}{k_3} \delta_1 - \frac{k_1}{k_3} \delta_2 - \frac{k_2}{k_3} \delta_3 \right)^2 \end{aligned} \quad (21)$$

The stability of the system is satisfied by the given conditions:

$$\begin{aligned} L_1 = L_2 = 1, L_3 = \frac{1}{2}, \\ L_4 = \frac{1}{2} \left(\frac{1}{k_3} \delta_1 - \frac{k_1}{k_3} \delta_2 - \frac{k_2}{k_3} \delta_3 \right)^2 \end{aligned} \quad (22)$$

As Eq. (21) has a negative sign, the system energy converges to zero with the time towards infinite and defines voltage control error converges as a compact set:

$$\delta = \left[\sqrt{\frac{L_4}{L_3}} \geq (V_{err} \mid V_{err}) \right] \quad (23)$$

2.4. Virtual impedance loop

The virtual impedance loop enhances system stability and damping and provides PQ decoupling. It also lowers the circulating current and power ripple. The virtual DG impedance value is determined from [50]. The voltage drop can be calculated in $\alpha\beta$ reference frame using Eq. (24) as stated:

$$\begin{bmatrix} V_{d\alpha} \\ V_{d\beta} \end{bmatrix} = \begin{bmatrix} R_1 & -\omega L_1 \\ \omega L_1 & R_1 \end{bmatrix} \begin{bmatrix} i_{0\alpha} \\ i_{0\beta} \end{bmatrix} \quad (24)$$

Here R_1 and L_1 represent the feeder impedance.

2.5. Droop control

Droop control is responsible for accurate power sharing among the distributed generations and lies at the upper level of primary control of

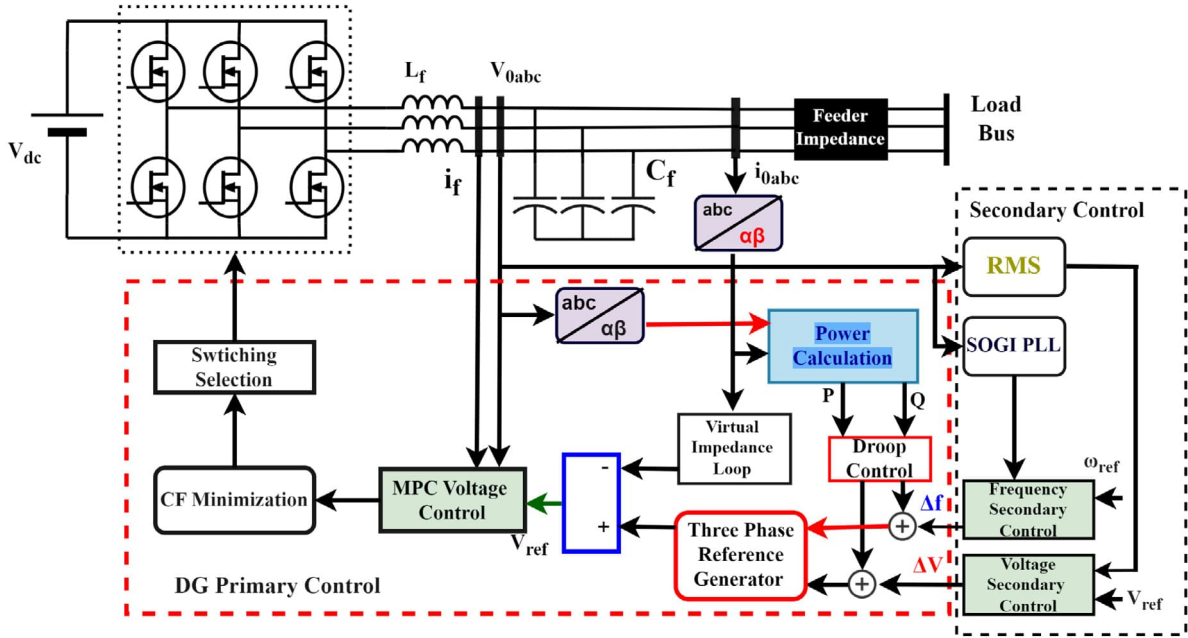


Fig. 6. Block diagram of the proposed decentralized control strategy.

MG, and is widely used due to its communication less structure [18,51]. P-f and Q-v droop strategy is implemented in this study and expressed as follows:

$$f = f_n - K_p(P - P_{ref}) \quad (25)$$

$$V = V_n - K_q(Q - Q_{ref}) \quad (26)$$

P_{ref} and Q_{ref} are zero in the case of islanded MG, and V and f are the voltage amplitude and frequency generated by the droop approach for concern DG. K_p and K_q are droop coefficients and expressed as $K_p = \frac{\Delta f}{P_{max}}$ and $K_q = \frac{\Delta V}{Q_{max}}$. ΔV and Δf are the maximum deviations in voltage and frequency, while P_{max} and Q_{max} are rated active and reactive power of the DG. Droop control keeps the voltage and phase angle stable, eliminating the circulating current. Eqs. (14) to (15) are used to evaluate the P and Q using instantaneous power theory in the $\alpha\beta$ reference frame:

$$P = i_{f\alpha}V_{0\alpha} + i_{f\beta}V_{0\beta} \quad (27)$$

$$Q = i_{f\alpha}V_{0\beta} - i_{f\beta}V_{0\alpha} \quad (28)$$

3. Secondary control

The fundamental responsibility of secondary control is to regulate the voltage and frequency deviation at PCC and forcefully shift the system variables to their nominal reference values with zero steady-state error after each change of generation and load. However, these deviations are generated due to overseeing the primary control. The voltage and frequency deviations are larger in the case of linear theory based controllers while smaller in the case of nonlinear controllers. In order to attenuate these deviations, the PI controller is used as a regulator. The secondary control layer usually consists of a voltage and frequency regulation loop. A second order generalized integrator phase locked loop (SOGI PLL) is used to measure the system's frequency. The secondary voltage and frequency compensation loops are extracted as follows:

$$\Delta V = k_{pv}(V_{ref} - V_{Act}) + k_{iv} \int (V_{ref} - V_{Act}) dt \quad (29)$$

$$\Delta f = k_{pf}(f_{ref} - f_{SOGI}) + k_{if} \int (f_{ref} - f_{SOGI}) dt \quad (30)$$

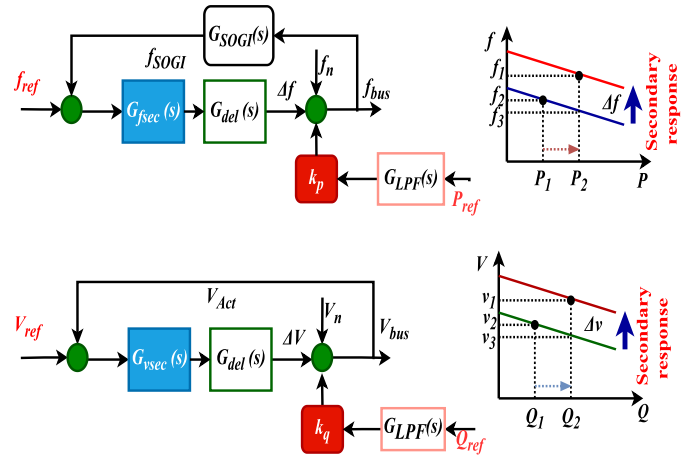


Fig. 7. Block diagram of the secondary control for frequency and voltage restoration.

where k_{pv} , k_{iv} , k_{pf} and k_{if} are the gain parameters of secondary layers regulators. V_{ref} and f_{ref} are the reference voltage and frequency of MG, while f_{SOGI} and V_{Act} are the actual frequency and voltage of AC bus in MG.

Fig. 7 illustrates the complete structure and process and how secondary control works and restores the voltage and frequency deviation. However, the response of the secondary level control is slower than the primary level control. As shown in the p-f graph, with the load increment, primary control acts first accordingly and increases the power generation. However, the system's frequency moves from f_2 to f_3 Hz. Then secondary control adds the δf factor into droop control to shift the characteristic curve to attain the system frequency. The same principle is applied in the voltage droop case. Without secondary control, the amplitude and frequency of MG would be load dependent. To design the regulator and analyze the system's stability, the transfer function is determined for the frequency regulation loop as written in Eq. (32). As shown in Fig. 6, the block model comprises droop control, secondary control gain, second order generalized integrator based phase lock loop, and communication delay. The block model is

mathematically represented as:

$$f_{bus} = \frac{G_{fsec}(s)G_{del}(s)}{1 + G_{fsec}(s)G_{del}(s)G_{SOGI}(s)} f_{ref} - \frac{k_p G_{LPF}(s)}{1 + G_{fsec}(s)G_{del}(s)G_{SOGI}(s)} P_{ref} \quad (31)$$

Here the transfer function is demonstrated as follows:

$$G_{fsec}(s) = \frac{k_{pf}s + k_{if}}{s} \quad (32)$$

$$G_{del}(s) = \frac{1}{(s + 1.5\omega_s)} \quad (33)$$

$$G_{LPF}(s) = \frac{\omega_c}{s + \omega_c} \quad (34)$$

The P_{ref} to f_{bus} transfer function can be written as:

$$f_{bus} = \frac{k_p \omega_c s (s^2 + sa + b)}{s^4 + s^3c + s^2d + se + f} P_{ref} \quad (35)$$

The parameters are given as:

$$a = t + 1.5T_s, \quad b = 1.5T_s t c = 1.5T_s + \omega_c + t \quad (36)$$

$$d = \omega_c (1.5T_s + t) + t (1.5T_s + k_{pf}) \quad (37)$$

$$e = t (\omega_c (k_{pf} + 1.5T_s) + k_{if}) f = tk_{if}\omega_c \quad (38)$$

By using this model, the secondary control parameters can be easily adjusted, and the effects of communication delays can also be analyzed. The voltage regulation loop is also modeled and developed using the same procedure.

4. Dynamics loads

The dynamic load is a load in which active and reactive power depends on the voltage and frequency of the systems. However, the voltage variation is in practice larger than the frequency variation [52]. The mathematical model of the load as a function of voltage is as follows:

$$P = P_0 \left[\frac{V}{V_0} \right]^{n_p} (1 + n_{pf} \Delta f) \quad (39)$$

$$Q = Q_0 \left[\frac{V}{V_0} \right]^{n_q} (1 + n_{qf} \Delta f) \quad (40)$$

P_0 and Q_0 are the nominal power rating of load. P and Q are the net power rating of load w.r.t the frequency and voltage of the system. The n_p and n_q are the load constants that define the load's nature. For constant current load, the value of n_p and n_q equals to one, and the value is two for constant impedance load. n_{qf} and n_{pf} are weighting factors to control the effect of frequency on load. The relationship between power and voltage is quadratic under constant impedance load (CZ), while in constant current load (CI), power is linear with bus voltage. However, constant power (CP) loads are independent of voltage. Table 4 expressed load constants, the power rating of the dynamic loads used in this study.

5. Simulation results

This part of the article discusses the simulation studies of the MG model developed in the MATLAB/Simulink environment to evaluate the performance of the proposed control strategy. Several MATLAB/Simulink simulations are carried out to assess the response of the proposed controller under different types of dynamic loads. In the simulation studies, two DGs with feeder mismatch are tested under different dynamic loads such as constant current, constant impedance, and constant power load to validate the performance of the studied controller, as shown in Fig. 8. The proposed system's control parameters

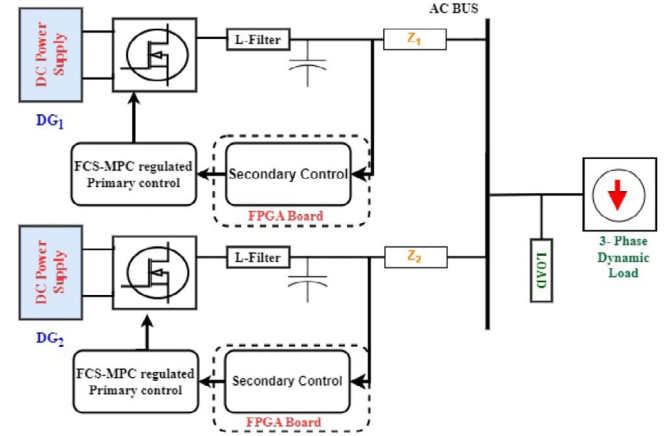


Fig. 8. Simulated communication and physical model of MG.

Table 4

Dynamics load contacts and their power ratings.

Load types	Load constants		Active power rating P_0 (kW)	Reactive power rating Q_0 (kVar)
	n_p	n_q		
Constant Current (CI)	1	1	6	4
Constant Impedance (CZ)	2	2	2	0
Constant Power (CP)	0	0	8	6
Industrial motor load	0.1	0.6	15	7

Table 5

Simulation parameters.

Parameter	Value
DC Input V_{dc}	700 [V]
Inductor value	$L_f = 2 \times 10^{-3}$ [H]
Nominal Bus Voltage	$V_{bus} = 320$ [V]
Capacitor	$C_f = 250 \times 10^{-6}$ [F]
System Frequency	50 [Hz]
Droop Coefficients	$K_p = 0.0001$, $K_q = 0.001$
Sampling Time	20×10^{-6} [s]
Secondary Voltage Control Gains	$K_p = 1.01$, $K_i = 0.001$
Secondary Frequency Control Gains	$K_p = 0.165$, $K_i = 0.001$
Switching Frequency	20 [kHz]
Line Impedance	$R_1 = 0.1$ [Ω], $L_1 = 2.4 \times 10^{-3}$ [H]

are prescribed in Table 5, and the sampling time of the simulation is 20 μ s. The results analysis is further divided into two parts; the first part explains the response of the studied controller with secondary and without secondary controller under normal RL load. The second part illustrates the system's performance under different types of dynamic loads.

To validate the performance of the proposed control, two DGs are operated in parallel, having an LC filter, and a feeder impedance is also added to make the system more realistic. The total load of 13 kW and 6 kVar is connected to the common MG AC bus. Fig. 9 shows the voltage and frequency of the DG_1 and DG_2 without secondary control. The initial part of the RL load of 9 kW and 4 kVar is suddenly connected to the system at instant $t = 0.2$ s. So, there is a negligible dip in the voltage and frequency due to connecting the initial load. Again, at instant $t = 0.6$ s, the load is further increased to 13 kW and 6 kVar. The DGs' voltage and frequency drop and settle at a lower value due to the absence of secondary control.

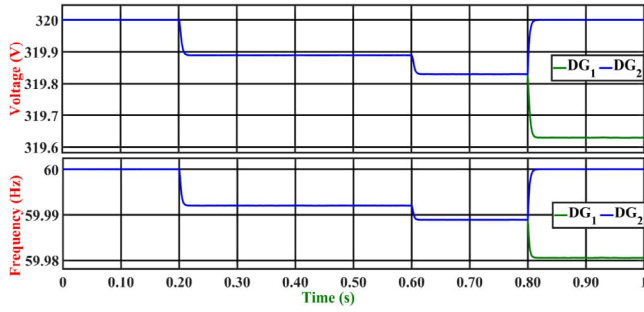


Fig. 9. Frequency and voltage of DGs under RL load, when secondary control is not employed.

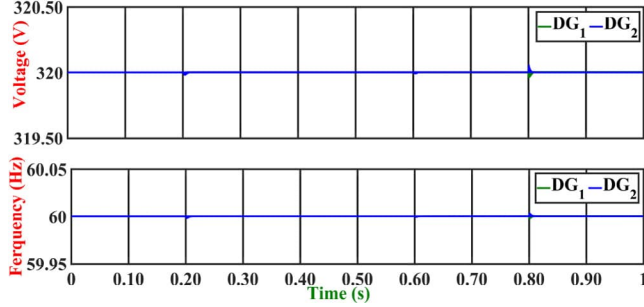


Fig. 10. Frequency and voltage of DGs under RL load, when secondary control is employed.

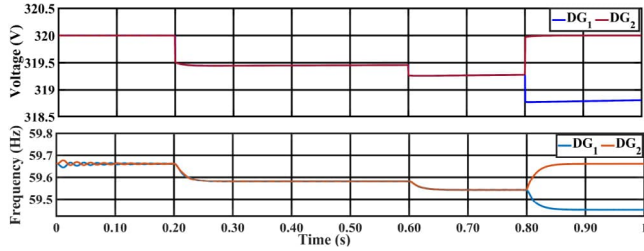


Fig. 11. Frequency and voltage waveform of DGs (PI based primary control) under RL load.

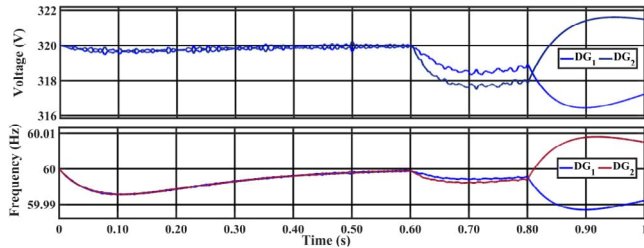


Fig. 12. Frequency and voltage waveform of DGs under RL load, when PI based hierarchical control is implemented.

At $t = 0.8$ s, the DG_1 is disconnected from the system. Therefore, the frequency of DG_2 drops from its nominal value, and the voltage also falls due to an increased share of the load. DG_2 is under a no load condition, so the voltage and frequency of DG_2 elevate to the predefined reference value.

Fig. 10 illustrates the voltage and frequency of the DGs with secondary control. It can be observed from Fig. 10 that the frequency and voltage demonstrate a slight dip and deviation from the reference values due to the load change. The secondary controller adds the increments to attain the reference value within no time. It is also seen

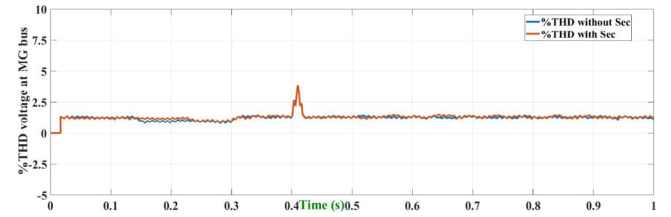


Fig. 13. THD of the MG at PCC.

in Fig. 10 that small transients occur in the system due to the operation of circuit breakers. However, the controller effectively accomplishes its goal of promptly achieving the reference voltage and frequency. Figs. 11 to 12 present DGs' output voltage and frequency when implementing PI-based hierarchical control. As shown in Fig. 11, the voltage and frequency of DGs decrease with the increase in load due to the absence of secondary control loop, and the PI based primary control loop has more deviation in voltage and frequency compared to the proposed controller. Fig. 12 depicts the performance of DGs when PI controller based hierarchical control is implemented. From Fig. 12, it can be observed that the PI based hierarchical control exhibits inferior performance when compared to the proposed control scheme. Fig. 13 illustrates the total harmonic distortion (THD) of the voltage at the AC bus of the MG. The voltage THD remains under 2 percent for the proposed control scheme.

The performance of the proposed PI+MPC based hierarchical control scheme is also analyzed under the different dynamics loads such as CZ, CI, and CP.

Constant Impedance: The output power of CZ load is in a quadratic relationship with voltage. Fig. 14(a) exhibits the voltage and frequency of DG_1 and DG_2 under constant impedance (CZ) load. At $t = 0.3$ s, the load of 2 kW is suddenly connected to the system. However, the voltage and frequency remain stable despite the switching of the load. The THD percentage of the current is 0.65. So the proposed controller effectively suppressed the voltage and current harmonics.

Constant Current: In this load, the output current remains constant, but the power changes linearly with the voltage. The power rating CI load is 6 kW and 4 kVar, which is connected to the system at $t = 0.3$ s, as demonstrated in Fig. 14(b). It is observed from the simulation results that the voltage and frequency of the system drop due to the addition of the load. But the proposed control system effectively tracks the reference and shares the DGs' harmonics. The percentage THD of the voltage is less than with the conventional control techniques, as shown in Table 6. At the same time, the current harmonics is about 0.47 percent, far less than the recommended value of IEEE/IEC standards such as IEC 62040, IEEE 1547 [53], and IEEE 519 [54]. The IEEE 519 standard recommends that the total harmonic distortion (THD) for voltage should not exceed 5 percent for systems with a voltage at the point of common coupling (PCC) of 69 kV and below. For individual harmonics, the standard recommends that it should not exceed 3 percent [54].

Constant Power: In this type of load, power remains constant and dependent on the input voltage change. The total load of 8 kW and 6 kVar is applied to the system at 0.3 s, as shown in Fig. 14(c). The system voltage and frequency show some disturbance, attain the reference, and become stable. The current harmonics are observed at PCC due to the feeder mismatch. However, the current harmonics are reduced and properly shared by the DGs. The current harmonic percentage is 0.33 at the PCC. The THD percentage comparison among the different control schemes is presented in Table 6.

Fig. 14(d) illustrates the simulation results of voltage and frequency of islanded MG when the industrial motor load is connected with a power rating of 16.55 kVA. The motor load is connected to the system at 0.3 s and shows the spike in voltage and current waveform due to the switching of the circuit breaker. The nominal voltage

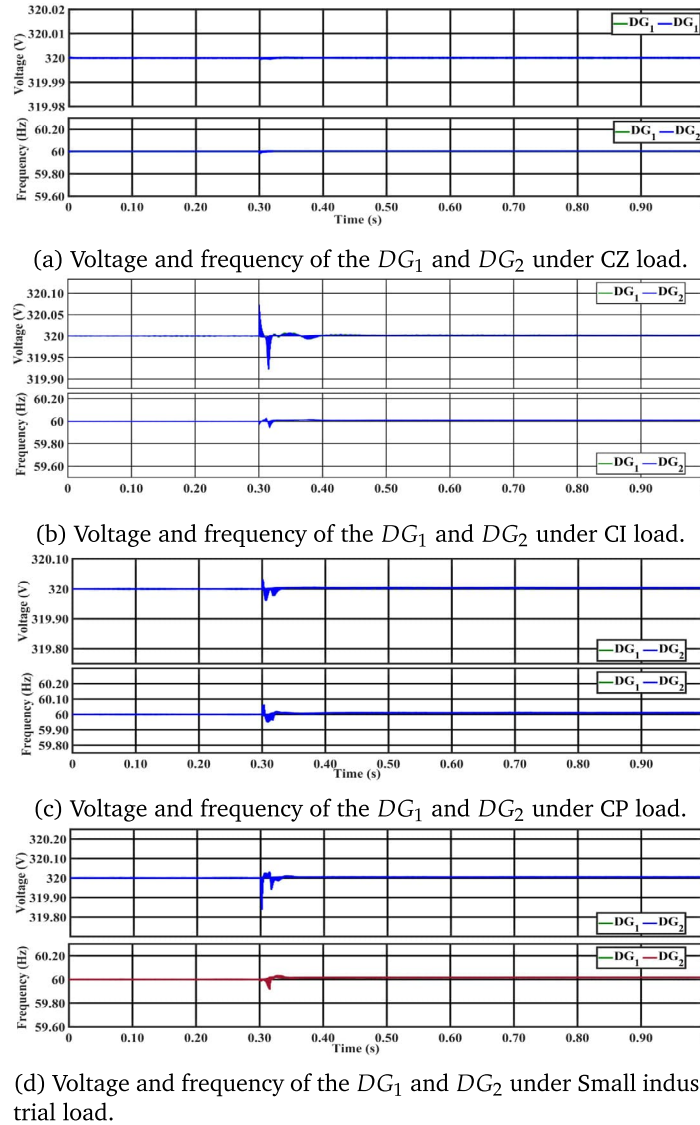


Fig. 14. Impact of different dynamics loads on the voltage and frequency of the AC MG.

and frequency of the DGs deviate from their reference. The proposed secondary controller eliminates voltage and frequency deviation with minor transients in 0.1 s, produced by the droop control due to a change in load. The current harmonics in the case of the industrial motor is 0.22 percent. The active and reactive power generated by the DGs to meet the load demand is illustrated in Fig. 15. The power voltage relation is quadratic in the case of CZ load and also has a large load power variation. At the same time, the CI load has less load power variation compared to CZ and has linear relation between voltage & power. In the case of CP, the voltage is not dependent on power and has a constant power load. Table 6 explains the performance analysis of THD among different control techniques. The proposed hybrid control scheme has achieved less percentage THD in all load types.

5.1. Controller-HIL studies

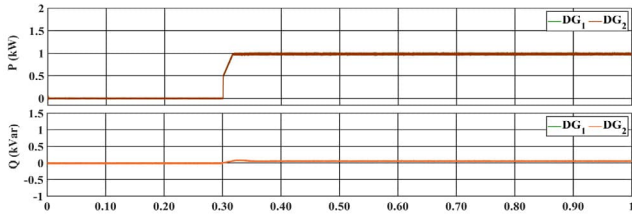
FPGA-in-the-loop (FIL) wizard provides the capability to use MATLAB/Simulink for testing controllers in real hardware conditions. The FIL wizard generates the code in VHSIC hardware descriptive language (VHDL) then generated VHDL code of the controller under test (CUT)

Table 6

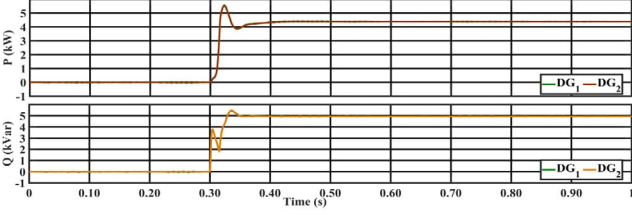
Voltage quality performance of the proposed controller under complex load conditions.

Load Types	Conventional PR based Hierarchical control (THD) [20,21]	MPC based Hierarchical control (THD) [21]	Proposed (THD)
Constant Current	7.10%	3.69%	0.98%
Constant Impedance	7.10%	3.69%	0.98%
Constant Power	7.10%	3.69%	0.98%

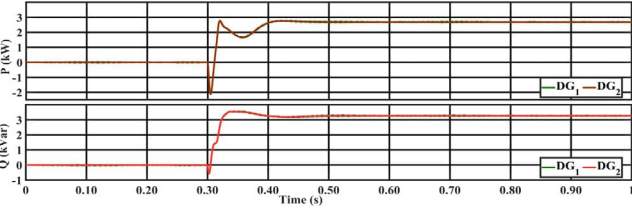
is burned on the selected FPGA board. The communication between the board and MATLAB/Simulink is carried out through a JTAG cable. In this study, ZYBO Z7 (ZYNQ-7020 development board) is used. The ZYBO Z7 is driven by 125 MHz oscillators and supports the JTAG mode. It has 13300 logic slices, 106,4000 flip flops, and 630 kB embedded RAM. Fig. 16 illustrates the working of the FIL implementation in



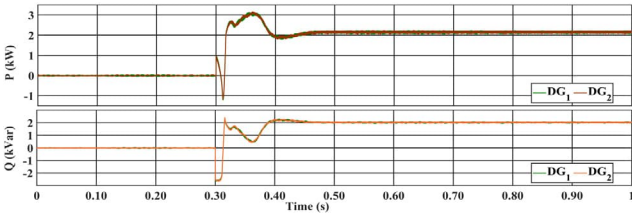
(a) Active and reactive power generated by DG_1 and DG_2 under CZ load.



(b) Active and reactive power generated by DG_1 and DG_2 under CI load.



(c) Active and reactive power generated by DG_1 and DG_2 under CP load.



(d) Active and reactive power generated by DG_1 and DG_2 under Small industrial load.

Fig. 15. The response of DGs power generation under different dynamic loads.

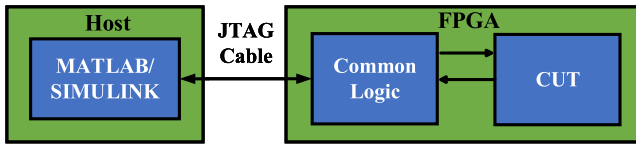


Fig. 16. Working principle of FPGA-in-Loop simulation environment.

SIMULINK. The CUT is burnt on the FPGA board, while the remaining AC MG model is on the MATLAB/Simulink environment. The interactive communication is done through a JTAG cable. FIL Implementation is performed in the following steps:

1. The controller under test is specified using a Simulink subsystem. Then inputs and outputs of the subsystem are defined as fixed data types (This operation can be performed using SIMULINK Fixed Point Tool).
2. After defining data types, select the CUT subsystem, open the HDL workflow, and run all tasks.
3. After running all tasks successfully, Matlab will generate the VHDL code of CUT and write it up on the FPGA board.

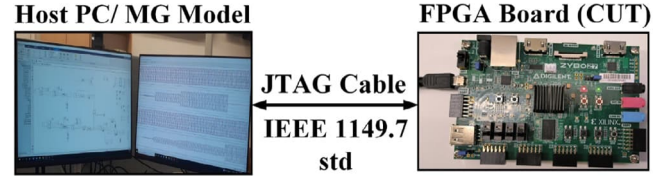


Fig. 17. Systematic view of FPGA controller hardware in the loop simulation environment along with the signal flow.

The performance of the studied controller is verified experimentally. Fig. 17 presents the systematic diagram of the experimental setup utilized for the proposed algorithm. This study implements the secondary controller on an FPGA card, while the AC MG model and MPC-based primary controller are modeled on MATLAB/Simulink environment. The controller hardware in the loop (CHIL) testing is carried out to study the response of the secondary controller in real time. Fig. 8 explains the detailed structure of the studied cases. Fig. 18 expressed the voltage and current of DERs during the step change of load under primary and secondary control. At $t = 0.2$ s, the RL load is connected to MG at the PCC. Voltage, the output current of the DERs remains stable despite a smaller dip, as shown in Fig. 18. Suddenly further load of 5 kW & 2 KVar is added into the system to see the impact of load on the proposed controller at $t = 0.6$ s. The system remains stable and attains the new power demand in no time. At $t = 0.8$ s, hot-swap operation is performed. Usually, this type of simulations studies is performed for UPS applications [55]. In this test, one DG suddenly goes out of the system due to a circuit breaker tripping. The remaining DGs take the whole connected load. It can be noticed from the figure that DG_1 instantly increased its power generation to fulfill the load demand. The quality of voltage and current remained stable despite the transition period when DG_2 was isolated from the system. Fig. 19 shows the voltage and frequency of the DGs. It is observed from Fig. 19 that the voltage and frequency of the system remain stable despite disturbances occurring to changes in load. Fig. 20 shows the response of droop control to share the active and reactive power between the DG_1 and DG_2 according to the load demand.

Figs. 21 to 22 present the system's fault study results. At $t = 0.3$ s, the three phase ground fault occurred at the PCC. DG voltage becomes zero, and the output current increases by 3 times the load current. Fig. 22 illustrates the fault current injection and bus voltage at the point of fault. When the fault is cleared at 0.4 s, the voltage and current of the MG are stabilized within no time.

5.2. Parametric uncertainty tests

This section discusses the performance of the proposed controller under the parameter uncertainty issues. The filter value of the DG is changed at $t = 0.4$ s from 2 mH to 1 mH. After changing the filter inductance value, The proposed controller performs better than PI, as shown in Figs. 23 to 24. This comparison is carried out based on THD in the converter's output voltage, which is 1.88 percent in the case of the proposed controller, but THD is 4 percent when PI is employed. The results illustrate the suitability and better performance of the studied controller under realistic conditions, and thus the proposed control can be effectively implemented for practical applications.

6. Conclusion

This paper proposed a decentralized hierarchical control comprised of FCS-MPC-based primary control and PI-based secondary approach for islanded AC microgrid to enhance the transient stability, load sharing, and power quality among the parallel connected DGs in AC MG under different dynamic loads (CZ, CI, CP, and industrial load). The mathematical stability of the proposed controller is also justified

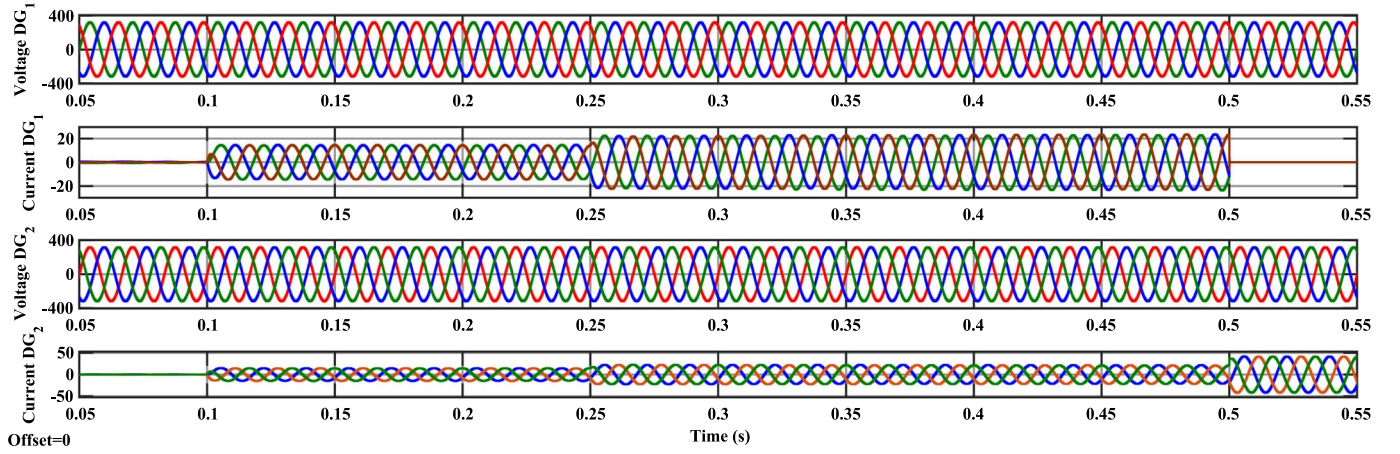


Fig. 18. Three phase voltage of DERs with RL load under step change of load.

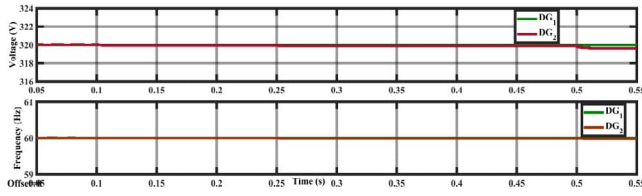


Fig. 19. DERs frequency and output voltage under step change of load.

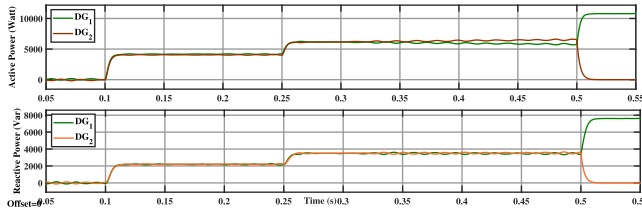


Fig. 20. Active and reactive power generated by the DERs to cope with the load demand.

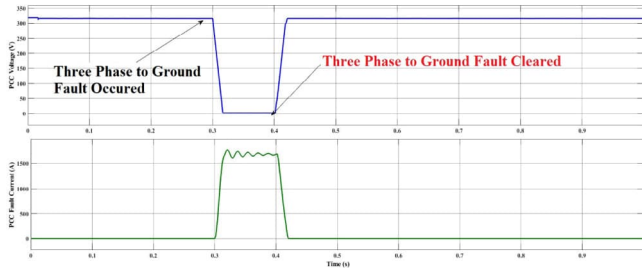


Fig. 21. Voltage and fault current injection during the 3-phase balanced fault at PCC.

using Lyapunov stability criteria. This rigorous mathematical proof confirms that the controller maintains stability within the system. The performance of the proposed control scheme is validated through the realistic MG test bench comprising two DGs operated in parallel along with an LC filter and a feeder impedance. The effectiveness of the proposed control technique was verified by performing simulations in MATLAB/Simulink along with hardware-in-loop testing using the FPGA-in-loop. The simulations and hardware setup results illustrated that the proposed approach tracked the reference with zero steady-state error by effectively regulating the voltage and frequency to its nominal value. The proposed control strategy achieved a THD (%)

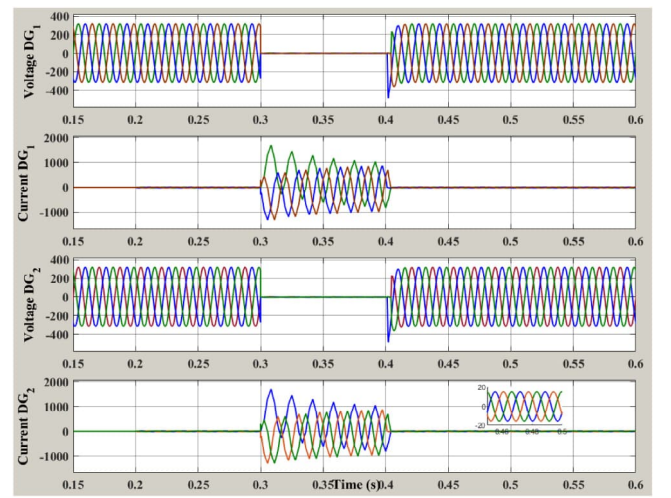
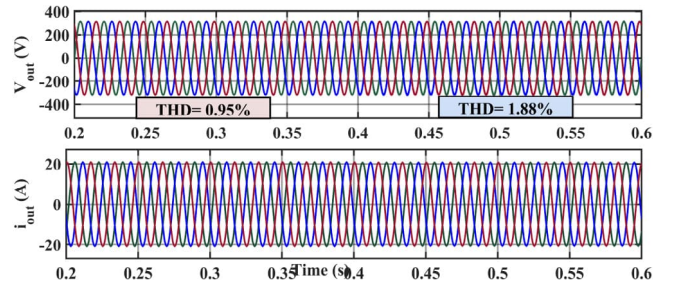
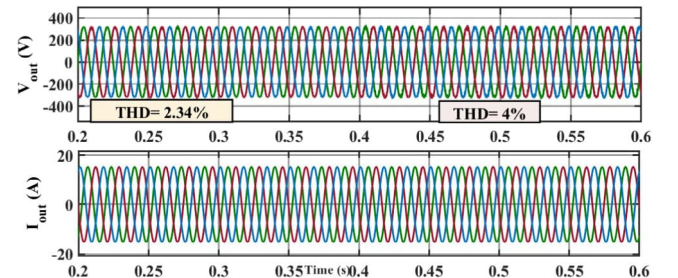


Fig. 22. Three phase voltage and output current of DERs under 3-phase balanced fault.

Fig. 23. Performance of the proposed control approach under load inductance changes $L = 2 \text{ mH}$ to $L = 1 \text{ mH}$ at $t = 0.4 \text{ s}$.Fig. 24. Performance of the PI control approach under load inductance changes $L = 2 \text{ mH}$ to $L = 1 \text{ mH}$ at $t = 0.4 \text{ s}$.

of 0.98 percent, much less than required per IEEE standards. Consequently, it enhances the power quality and ensures active and reactive power sharing between the DER under steady-state and transient load conditions.

CRedit authorship contribution statement

Hussain Sarwar Khan: Conceptualization, Methodology, Software & Hardware implementation, Writing – original draft. **Kimmo Kauhaniemi:** Supervision, Proofreading, Modification for the final layout.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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