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A High Gain AC-DC Rectifier Based on Current-Fed Cockcroft-Walton Voltage Multiplier for Motor Drive Applications

Ahmad Zarepour [1], Amirhossein Rajaei [1,*], Hooman Mohammadi-Moghadam [1] and Mahdi Shahparasti [2]

[1] Department of Electrical Engineering, Shiraz University of Technology, Shiraz 71557-13876, Iran; a.zarepour@sutech.ac.ir (A.Z.); hw.mohammadi@gmail.com (H.M.-M.)
[2] Flexible Energy Resources, School of Technology and Innovations, University of Vaasa, 65200 Vaasa, Finland; mahdi.shahparasti@uwasa.fi
* Correspondence: a.rajaei@sutech.ac.ir

Abstract: This paper proposes a novel high-gain AC-DC converter based on the Cockcroft-Walton (CW) voltage multiplier which can be utilized in motor drive systems with low input voltage. In this topology, use of the voltage multiplier and boost circuit results in the increment of converter gain which has a significant impact on the cost and efficiency of the system. Moreover, in this converter, the AC voltage is directly changed to DC voltage using the switching method in high frequency and, as well, the power factor is corrected. Besides, this high-frequency converter contributes to the reduction of output ripple. On the other hand, cost efficiency, the low voltage stress on capacitors and diodes, compactness, and the high voltage ratio, are achieved from the Cockcroft-Walton circuit. Furthermore, the hysteresis method is presented for converter switching to correct the power factor. The converter is simulated in MATLAB software to demonstrate the effectiveness of the suggested method. Lastly, a laboratory prototype of the suggested converter is built, several tests are done in order to verify the theoretical analysis, and comprehensive comparison with the state-of-the-art converter is done.

Keywords: AC-DC converter; high voltage ratio; Cockcroft-Walton multiplier; rectifier; power factor correction

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1. Introduction

Nowadays, high gain AC/DC converters are widely used in manufacturing, research, medicine, and the military, such as laboratory devices, X-ray facilities, dust screening, insulation inspection, and electrostatic coating [1–4]. In other applications, such as a motor drive, the system consists of an inverter for controlling the motor and a typical type of rectifier for changing the AC to DC voltage. In addition, in this structure, the DC voltage must be higher than 1.63 times the motor voltage; therefore, a high gain rectifier must be used to boost the AC input voltage in case of feeding through a low voltage source. Sustainable renewable energy sources are new energy systems that are widely used to meet the growing energy needs of today and tomorrow. In order to use the variable generated power by renewable power plants, employing a high-performance interface system is inevitable. As an example, the interface system for a wind energy power plant includes two parts:

- Generator: generates electric power from mechanical energy. Several types of generators such as induction, synchronous, and permanent magnet (PM) generators are used;
- Power interface system: regulates voltage and current and transfers energy from generator to the power grid or standalone load.

Due to the low output voltage of generators and most other renewable energy systems, high step-up converters are widely used as a part of interface systems to achieve better

performance and higher efficiency. In this paper, we have introduced a new structure of an AC-DC high step-up converter which can be used as a power electronic interface for renewable energy systems.

Traditional converters such as current source converter (CSC) and voltage source converter (VSC), which are normally used in most industries, have several disadvantages. Disadvantages are that (1) the main switching component of VSC and CSC are not interchangeable, (2) they operate as a boost or buck converter only, (3) to have a multi-functional DC/AC converter, a DC-DC converter and VSC must be combined which leads to lower reliability, and (4) being exposed to the EMI phenomenon and the components in either short or open circuit mode causes detriment. Therefore, the range of output voltage is restricted in comparison to the input voltage. In addition, Z-source inverters include the whole range of power conversion applications, and they have some benefits, such as removing switches which are normally needed at the boosting point for increasing stability due to not being sensitive to shoot-through. Although, they usually involve higher voltage level switches [5]. In [6–9], researchers have thoroughly studied DC-DC converters with high turn ratio transformers that are isolated. While they have galvanic insulation that is critical for many applications, their disadvantages are their large parasite efficiency and high-turn-ratio transformer leakage inductance, which induces high current spikes and high voltage on semi-conductor components. Because of its essential property, the Switched-Capacitor Converter has drawn attention because it requires no magnetic part contribution [10,11]. Compared with conventional inductor-based converters, this feature allows it to achieve higher power density and complete monolithic mixture [12–14]. The important disadvantage is that it carries restricted control capacity and pulsating feedback current, which is cause for concern [15].

The controllable output AC-DC converters are employed for use in DC-AC and DC-DC converters. Because of severe regulation on conducted electromagnetic interference, passive and active power factor correction is required [16]. Multiple switches in inverter systems are often employed in bi-directional power flow, among different PWM rectifications. Such converters exhibit appropriate output regarding the total harmonic distortion of input current, efficiency, and power factor due to the pulse width modulation function. Multiple PWM rectifiers involve a complicated controller and require safety against the failure of switching equipment [17]. Also, the harmonic current injection approach is employed in large three-phase rectifier systems for power factor enhancement and correction of input current. Harmonic injection strategies involve the injection of a different or related DC source to produce a harmonic current, and also in order to alter the duty cycle of the rectifier switch, and a suitable voltage is used in the control procedure [18,19]. The suitable input filter reduces the converter's performance. Regarding this, Vienna rectifiers are common converters, in which three switches control current waveforms at the input side. Vienna rectifiers are studied with their initial and updated topologies, and, as well, a closed-loop Vienna rectifier has been observed providing reasonable output with boost voltage gain [20–29]. The traditional rectifiers are durable and inexpensive; however, they draw reactive power or non-sinusoidal currents from the source, which reduces the efficiency of the component. Power factor correction (PFC) or passive linear filters topologies may be utilized to counteract harmonic distortion caused by regular rectifiers [30–32]. The three-phase multi-pulse rectifiers gain harmonic cancellation by the addition of a three-phase transformer using phase shift. In fact, the diode rectifier's simplicity and durability characteristics are retained; although, they are heavy, voluminous, and costly [33,34]. Benefiting from high-frequency switching technology, several improved CW circuits have been developed to save transformer volume, as well as controlling the output voltage and reducing output ripple. Voltage-fed modified CW topologies were proposed in [35–37], which prepare ease of implementation as well as a high voltage gain. However, in such structures, the high-frequency transformer with lower turn ratios induces the inductance of leakage and large winding efficiency, resulting in higher switching losses on the switch and heavy current and voltage pressures. The key problems associated with CW-VM

are the current-dependent voltage drop and the voltage ripple, which can deteriorate converter output, particularly for those with a large number of stages. To solve these issues, a variety of improvements have been suggested, such as the use of a current-fed system [38,39]. In addition, the current-fed Capacitor diode voltage multipliers (CD-VM) system is a viable alternative that might be employed for the boosting stage of low-voltage renewable energy capital control electronic interface. Among different forms of CD-VM, the most common circuit is half-wave (CW-VM) [40,41]. The standard Cockcroft-Walton (CW) voltage multiplier offers the benefits of cost-efficiency, a low voltage stress on capacitors and diodes, and a high voltage ratio. A CW voltage multiplier is designed in every stage using cascading multiple diode-capacitor stages that have two diodes and two capacitors. Further, ref. [42] presents an analytical design procedure for RF energy harvesting systems using the CWVM structure. As well, ref. [43] analyzed the operation principles of an *n*-stage current-fed Cockcroft-Walton (CF-CWVM) during transient and steady-state operations. The derived relations can be used for further explanation of the converter behaviour as well as a non-linear controller design. A design of high-voltage multipliers to generate underwater shockwaves is also described in [44].

In this article, a novel high-step current-fed rectifier has been introduced that uses a current-fed CW-VM, and also has two inductors and four switches. The low voltage tension on the switches allows low voltage MOSFETs to be used to increase both performance and reliability. Moreover, this article has been organized as follows. In Section 2, the steady-state analysis is presented. Section 3 discusses design considerations of the converter, and its control system is presented in Section 4. In Section 5, the simulation and experimental results that allowed us to validate the performance of the proposed converter are presented. Lastly, the conclusions of the proposed work are demonstrated in Section 6.

2. Steady-State Analysis

The suggested topology chiefly consists of a cascaded one-phase converter along with a conventional three-stage Cockcroft-Walton voltage multiplier, as seen in Figure 1. The single-phase converter is built with four bidirectional switches, separated into four denoted sets as S_1, S_2, S_3, and S_4. The proposed converter is invigorated to boost operation using the line-frequency AC source with a series inductor.

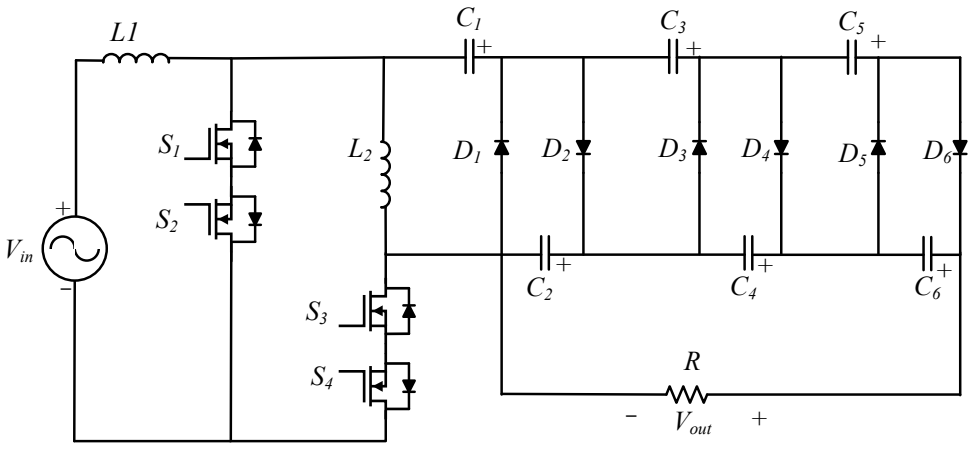


Figure 1. Circuit diagram of the proposed AC-DC rectifier.

The following hypotheses are assumed for the study of the suggested converter's steady-state behaviour:

1. The whole capacitors in the Cockcroft-Walton voltage multiplier are big, and every capacitor's voltage drop and ripple could be ignored under a suitable load condition;
2. The whole circuit elements are ideal, and the system is without power loss;
3. The suggested converter operates in continuous conduction mode (CCM), and also in the condition of a steady-state;

4. Ignoring safe commutation states (overlap time);
5. All values of capacitors are equal.

According to [7,20,21], the voltage ratios of capacitors are equal to:

$$V_{Ck} = \begin{cases} V_o/N & for\ k = 1 \\ 2V_o/N & for\ k = 2, 3, \ldots, N \end{cases} \qquad N = 2n \ . \tag{1}$$

In relation (1), N is the number of circuit layers that multiplies the CW voltage and V_o is the circuit's output voltage. Also, V_{Ck} is the k_{th} capacitor voltage. In the CW multiplier circuit, the output voltage is similar to the sum of the voltages of the series capacitor connected to the multiplier and is equal to:

$$V_o = V_{C2} + V_{C4} + V_{C6} + \ldots + V_{Ck}. \tag{2}$$

As voltages of all capacitors are the same except for the first capacitor, the output voltage of CW multiplier circuit is equal to:

$$V_o = nV_{Ck} = NV_{C1} = NV_\gamma, \tag{3}$$

where V_γ is the input voltage of the CW circuit.

The performance of the CW multiplier circuit will be investigated in two modes: negative and positive half-cycle of input voltage. In the positive half-cycle, S_2 and S_4 switches are off and the S_1 and S_3 switches are in switching mode. The circuit in the positive half-cycle is analysed in two modes.

In the first state, when the S_1 switch is on, the S_2, S_3, and S_4 switches are off; also, L_1 inductor current passes through the S_1 and S_2 switches, then the L_1 inductor is charged, and its current increases. During this period, the L_2 inductor supplies and discharges the CW multiplier current, in the CW current flow in Figure 2, respectively, and is at the positive half-cycle. In this case, the voltage across the inverter L_1 is equal to:

$$V_{L1} = v_{in}, \tag{4}$$

where v_{in} and V_{L1} are the input voltage and the voltage across L_1 inductor, respectively, and the inductor voltage L_2 is equal to:

$$V_{L2} = -V_{C1} = -\frac{V_o}{N}, \tag{5}$$

and capacitor current C_1 is in the opposite direction of I_{L2} current.

$$i_{C1} = -i_{L2}. \tag{6}$$

The second state also occurs in the positive half-cycle, while S_1 is turned off and the S_3 switch is turned on; S_2 and S_4 switches are still off. In this case, the L_1 inductor current is injected into the Cockcroft-Walton multiplier circuit as well as the L_2 inductor. Therefore, the L_1 inductor is discharged and the L_2 inductor is charged, which is shown in Figure 3, respectively, in the positive half-cycle.

In this switching interval, V_{L1} is equal to:

$$V_{L1} = v_{in} - V_{C_2} + V_{C_1} = v_{in} - \frac{V_o}{N}, \tag{7}$$

and the voltage of the inductor L_2 (V_{L2}) is equal to:

$$V_{L2} = -V_{C_1} + V_{C_2} = \frac{V_o}{N}, \tag{8}$$

also, the current of capacitor C_1 (i_{C1}) is achieved as follows:

$$i_{C1} = i_{L1} - i_{L2}. \tag{9}$$

the same analysis can be done for the negative half-cycle in two cases.

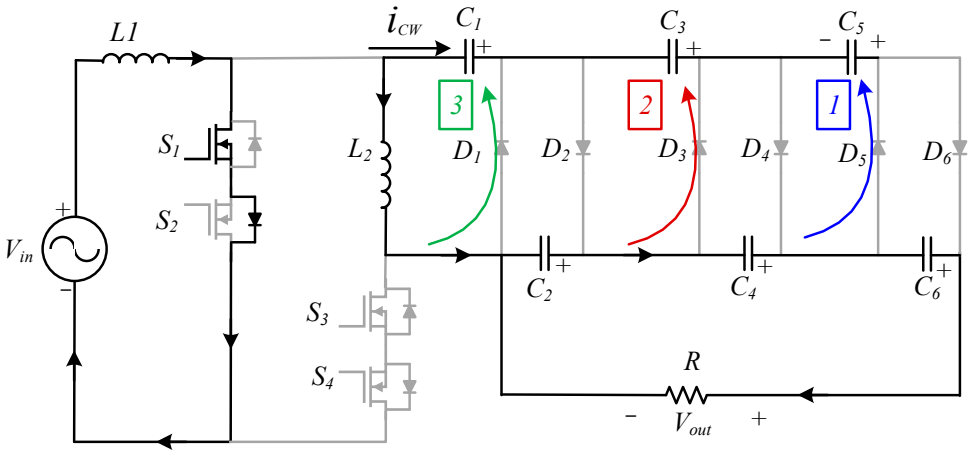


Figure 2. The conducting path of the converter current provided in the positive half cycle in the first state (The conduction mode begins with D_5 and propagates in an orderly manner to D_3 and D_1).

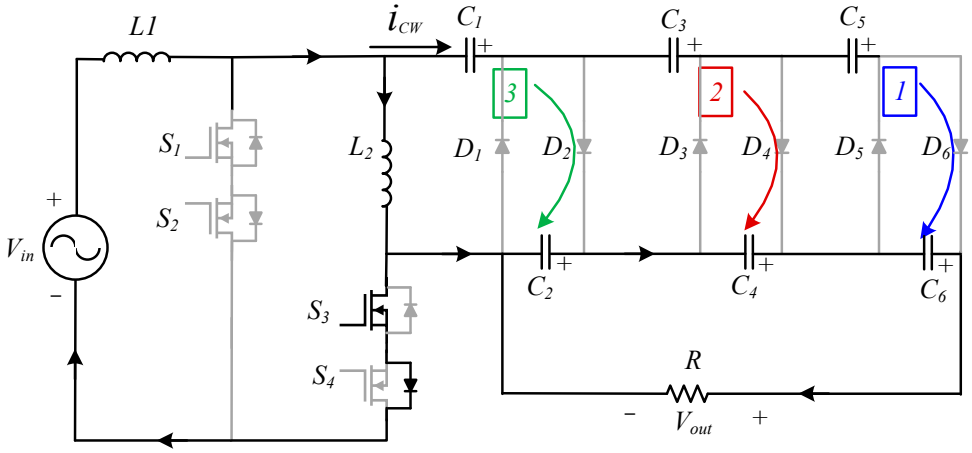


Figure 3. The conducting path of the converter current provided in the positive half-cycle in the second state (the conduction mode begins with D_6 and propagates in an orderly manner to D_4 and D_2).

The third state occurs when the S_2 switch is on, the S_1, S_3, and S_4 switches are off, the current of inductor L_1 passes through the S_1 and S_2 switches, and then the inductor L_1 is charged in the negative half-cycle, increasing its current. During this period, the L_2 inductor supplies and discharges the current of the CW multiplier, which is demonstrated in Figure 4, respectively, in the negative half-cycle.

The fourth state occurs in the negative half-cycle while the S_2 switch is off and the S_4 switch is on, and the S_1 and S_3 switches are still off. In this case, the L_1 inductor's current is injected into the Cockcroft-Walton multiplier circuit and is discharged. Then, the L_2 inductor is charged, which is shown in Figure 5, respectively, in the positive half cycle.

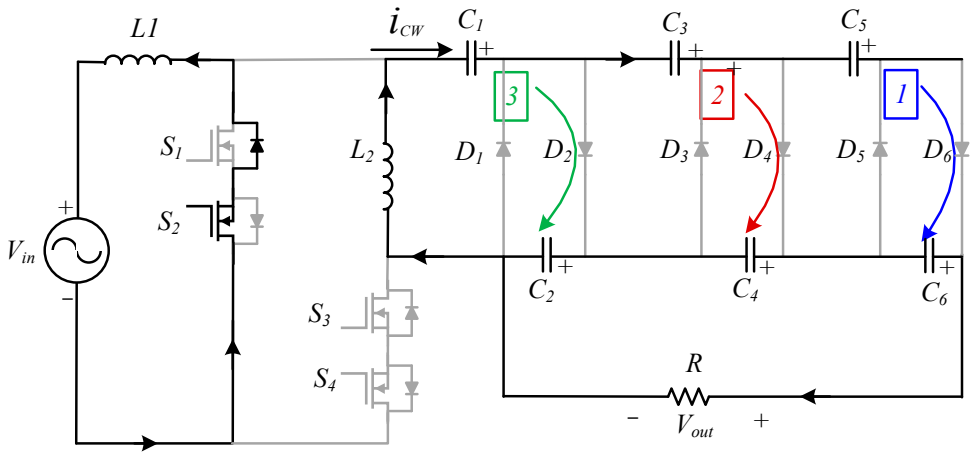


Figure 4. The conducting path of the converter's current provided in the negative half-cycle in the third state (the conduction mode begins with D_6 and propagates in an orderly manner to D_4 and D_2).

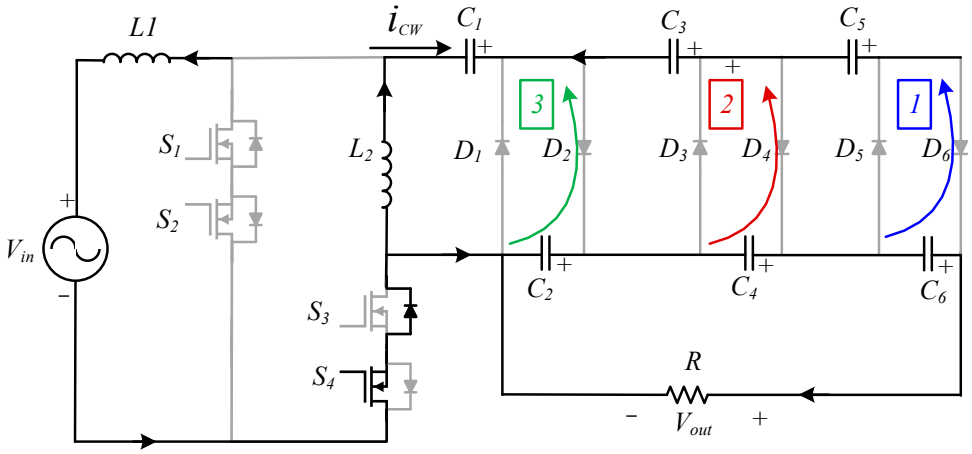


Figure 5. The conducting path of the converter current provided in the positive half cycle in the second state (the conduction begins with D_6 and propagates in an orderly manner to D_4 and D_2).

The converter analysis is carried out for the negative and positive half cycles similar to each other. Applying the rules of the average capacitor's current in a period, and using Equations (6) and (9), we have:

$$< V_{C_1} >= 0, \tag{10}$$

$$-i_{L2}DT_{SW} + (i_{L1} - i_{L2})(1 - D)T_{SW} = 0, \tag{11}$$

$$i_{L2} = (1 - D)i_{L1}. \tag{12}$$

The current ripple for L_1 inductor's current during $0 < t < DT_{sw}$ is calculated as:

$$\Delta i_{L1} = \frac{v_{in}}{L_1} DT_{SW}. \tag{13}$$

The T_{SW} is defined as the switching period and the D is defined as the duty cycle. The current ripple during this interval $((1 - D)\, T_{SW})$ is equal to:

$$\Delta i_{L1} = \frac{v_{in} - \frac{V_o}{N}}{L_1}(1 - D)T_{sw}. \tag{14}$$

Regarding the switching frequency, that of $1/T_{SW}$ is very high (about 150 kHz), and it can be assumed that the amount of charge and discharge of L_1 inductor is equal in the

switching period as well as that the average current during a T_{SW} period must be zero, and therefore, we have:

$$\frac{v_{in}(t)}{L_1} D T_{sw} + \frac{v_{in}(t) - \frac{V_o}{N}}{L_1}(1 - D) T_{sw} = 0, \tag{15}$$

$$v_{in}(t) = \frac{V_o}{N}(1 - D), \tag{16}$$

$$\frac{V_o}{v_{in}(t)} = \frac{N}{1 - D}, \tag{17}$$

where Equation (17) shows the relationship between output and input voltage. Assuming that output power is equal to the input power of the CW circuit, then:

$$V_o I_o = V_{in_{RMS}} I_{in_{RMS}}, \tag{18}$$

where V_{inRMS} and I_{inRMS} are the RMS values of input voltage and current, respectively. It should be noticed that the converter can be controlled in such a way that input current and voltage are in the same phase (converter conditions of power factor correction). Assuming resistance load, the value of output current is equal to:

$$i_{L1,\max} = \frac{\sqrt{2} P_o}{V_{in_{RMS}}} = \frac{\sqrt{2} V_o^2}{V_{in_{RMS}} R_o}, \tag{19}$$

where P_o, R_o, and V_o are defined as output power load resistance and output voltage, respectively. Also, the relationship between duty cycle D and instantaneous angle (ωt) is determined by Equation (20) and plotted in Figure 6.

$$D(t) = 1 - \frac{V_{in} N}{V_o} \sin(\omega\, t_3). \tag{20}$$

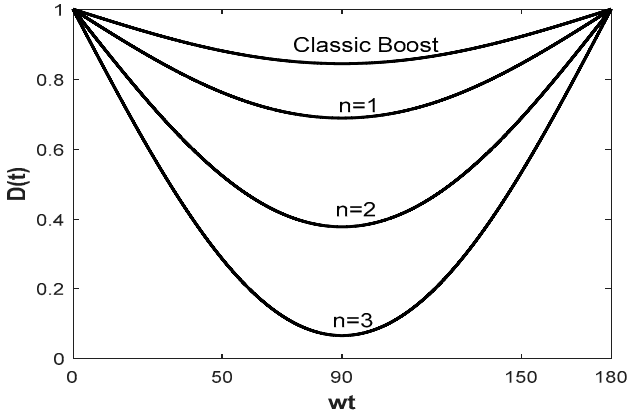


Figure 6. Relationship between D and ωt.

Regarding Figure 6, the value of the duty cycle in this converter is not constant and changes with time, and where the input voltage obtains its peak value, the duty cycle obtains its minimum value; also, while input voltage reaches the maximum value, the converter's switching frequency increases and the duty cycle changes in each half-cycle, and it is symmetric with respect to t_w = 90. Furthermore, the number of CW converter stages increases and the duty cycle changes in one-half cycle. This also shows the changes in the duty cycle of the boost converter, and the traditional boost converter in the duty cycle provides a higher duty than the output voltage converter provided. Figure 7 illustrates the voltage and current of switches the state of the converter in different scenarios.

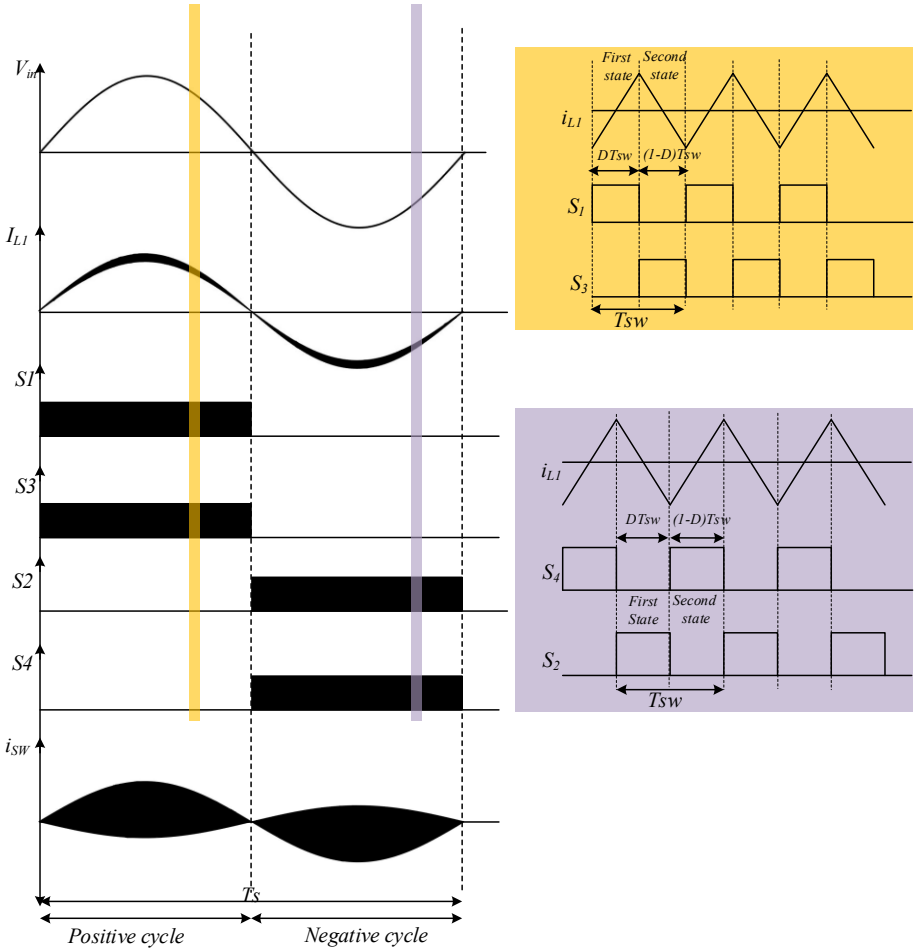


Figure 7. The waveforms of voltage, current, and switching cycle.

3. Design Considerations

3.1. Components Determination

In general, it is vital to specify the minimum values of capacitors and inductors based on current and voltage ripples, as well as current and voltage stresses of semiconductors to construct a power electronic converter. In this section, the parameters listed in Table 1 will be used to design the converter.

Table 1. Required parameters for converter design.

Symbols	Definitions	Values
$V_{in\ (rms)}$	Input voltage	220 V
$V_{out\ (DC)}$	Output voltage	1200 V
P_{out}	Output power	1000 W
R	Output resistance	1440 Ω
f_s	Maximum switching frequency	150 kHz
f_n	Line frequency	50 Hz

First, we try to calculate the L_1 inductor's value. The maximum input current value of the circuit is equal to:

$$i_{L,\max} = \frac{\sqrt{2}P_o}{\eta v_{in,rms}} = \frac{\sqrt{2} \times 1000}{0.9 \times 220} = 7.142A, \quad (21)$$

where η is the converter efficiency. The relationship between voltage and current of the inductor can be described as follows:

$$V_{L1} = L_1 \frac{\Delta i_{L1}}{\Delta t}, \tag{22}$$

$$L_1 = \frac{V_{L1}\Delta t}{\Delta i_{L1}}, \tag{23}$$

$$L_1 = \frac{v_{in}(t)D(t)T_{SW}}{K_i I_{L,\max}} = \frac{V_{in,RMS}\sqrt{2}\sin(wt) \times [1 - (\frac{V_m\sqrt{2}N}{V_o}\sin(wt))]T_{SW}}{K_i I_{L,\max}}. \tag{24}$$

The K_i value is the peak–peak change coefficient of the inductor's current, which is 0.05 times the input current, and then:

$$\begin{aligned} &\frac{dL_1}{dt} = (\frac{v_{in}(t)D(t)T_{SW}}{K_i I_{L,\max}})' \\ &\quad = (\frac{V_{in,RMS}\sqrt{2}\sin(\omega t)\times[1-(\frac{V_{in,RMS}\sqrt{2}N}{V_o}\sin(\omega t))]T_{SW}}{K_i I_{L,\max}})' = 0, \\ &\to \sin(\omega t) = \frac{1}{2\frac{V_{in,RMS}\sqrt{2}N}{V_o}} \to \omega t = \sin^{-1}(\frac{1}{2\frac{V_{in,RMS}\sqrt{2}N}{V_o}}) = 74.63^o. \end{aligned} \tag{25}$$

According to the relations (21) and (22), the value of L_1 = 2.8 mH is achieved.
Then, for calculating the L_2 inductor value, we have:

$$\begin{aligned} &i_{L2} = (1-D)i_{L1} \overset{(10)}{\to} i_{L2} = (\frac{V_{in}N}{V_o}\sin(\omega t))(I_{L1,\max}\sin(\omega t)) \\ &\to i_{L2} = \frac{V_{in}NI_{L1,\max}}{V_o}\sin^2(\omega t). \end{aligned} \tag{26}$$

The maximum value of I_{L2} occurs at ωt = 90 with respect to the relation (26); therefore, the maximum value of I_{L2} is equal to:

$$i_{L2,\max} = \frac{V_{in}NI_{L1,\max}}{V_o} = 2.61A. \tag{27}$$

Therefore, the value of L_2 is equal to:

$$L_2 = \frac{V_{L2}\Delta t}{\Delta i_{L2}}, \tag{28}$$

$$L_2 = \frac{\frac{V_o}{N}D_{\max}T_{sw}}{0.1 i_{L2,\max}} = 9.7mH. \tag{29}$$

The capacitor value in the Cockcroft-Walton converter is achieved by the ripple of the suitable output voltage. The voltage ripple and drop related to each capacitor could be achieved under the steady-state using the charging–discharge behaviours of capacitors. The K_{RF} is output voltage ripple coefficient, and if it is considered as $\frac{\Delta V_0}{V_o} < 0.1$, then the value of capacitor C_2 is calculated as follows:

$$C_2 > \left|\frac{T_{sw}I_o}{2V_oK_{RF}}[\frac{4NI_o}{\omega}(\frac{T_{sw}}{4} - \frac{4NV_m}{3_sV_o}) - 1]\right| \to C_2 > 374.3\ \mu\text{F}. \tag{30}$$

In addition, it is clear that if the capacitor value in the multiplier circuit is higher, then the output ripple of the circuit is lower; therefore, the 470 μF capacitors are used for the converter and other capacitors are chosen with the same value.

3.2. Voltage and Current Stress of Components

- **S_1, S_2, S_3, S_4 switch**

The highest current passing through these switches is equal to the highest input current. According to (21), the maximum current passing through these switches is 7.142 A, and regarding the operation of the circuit when these switches are off, the input voltage of the CW multiplier circuit falls on these switches. The amount of voltage stress on these switches depends on the number of stages of the CW circuit. For a converter with one stage, the highest voltage stress on these switches is equal to 600 V.

- **Diodes**

All the diodes in the steady-state operation convey similar charge over the period, i.e., similar average current. Consequently, since I_{L1} is equal to the average half-wave input current of the CW converter, the average current flowing in all diodes can be calculated during period T [38]:

$$I_D = \frac{i_L}{n}. \tag{31}$$

- **Capacitors**

In an n-stage Cockcroft-Walton circuit, given that the capacitors are large enough, all capacitors ideally maintain similar voltage except the first one, which has half the others. Consequently, the voltage stress on each capacitor is V_o/n, except for C_1, where the voltage stress is achieved as $(1 - D)\ V_o/n$.

Voltage stress on capacitor C_2 is achieved as 1260 V, and the voltage stress on capacitor C_1 will be equal to 660 V for K_{RF} = 0.1 based on (1).

- **The number of n-stage**

It is necessary to consider, in using Cockcroft-Walton, that the number of diodes enlarges to grow the DC gain by increasing n, and, thus, conduction loss of diodes will increase. This could lead to a reduction in overall performance. However, it is necessary to know that a lower number of n would result in higher voltage stress on the MOSFETs (need MOSFET with higher voltage rating) and, also, would result in increased power loss (conduction and switching) of MOSFETs. Hence, the trade-off between power loss of MOSFET and diodes must be performed in order to retrieve a suitable number of n. In practice, the converter is not ideal and has parasitic elements that cause the converter to have losses and decreases the converter voltage compared to the ideal condition.

3.3. Effect of Non-Idealities Components

The results of parasite elements on the suggested converter are investigated to achieve suitable comparability and practical insight. The parasitic elements that are discussed can be defined as: on-state resistance of switches R_{on}, forward voltage of the diodes V_D, and winding resistance R_{L1} and R_{L2}. According to these elements, the converter main losses are as follows:

- Losses due to switches;
- Losses due to inductor resistance;
- Losses due to diodes.

Power switch losses are divided into two types of switching losses and conduction losses. The conduction losses for the switches are equal to:

$$\begin{aligned} P_{loss,f} &= R_{on} {I_{sw,RMS}}^2 = P_{cond(s1,s2)} = R_{on}\left(i_{L1,\max}\sqrt{\tfrac{1}{2} + \tfrac{3N^2V^2_{in}}{8V_o^2}}\right)^2, \\ P_{cond(s3,s4)} &= R_{on} {i^2}_{L1,\max}\left(\tfrac{NV_{in}\sqrt{6}}{4V_o}\right)^2. \end{aligned} \tag{32}$$

and the switching loss is equal to:

$$P_{loss,sw} = \frac{1}{2} f_{sw} V_{SW} I_{SW} [t_{on} + t_{off}], \tag{33}$$

$$t_{on} = t_{ri} + t_{fv}, \tag{34}$$

$$t_{off} = t_{rv} + t_{fi}, \tag{35}$$

t_{ri} is the time interval of the switch transition from zero voltage to the nominal value and t_{fv} is the time interval of the switch transition from the nominal value to zero. t_{fi} is equal to the time duration that it takes for the switch to flow from the nominal value to zero and t_{rv} is for the time duration that it takes for the switch voltage to go from zero to the nominal value.

The loss of the inductors depends on their resistance as well as the current that passes through them:

$$\begin{aligned} P_{cond,L1} &= R_{L1} I^2_{L1,RMS} = R_{L1} I^2_{in,RMS}, \\ P_{cond,L2} &= R_{L2} \left[\tfrac{V_{in} N \sqrt{6}}{4 V_o} i_{L1,\max}\right]^2. \end{aligned} \tag{36}$$

Moreover, diodes have two types of loss. Diode conduction losses and loss of diode relate to the on and off.

The conductive losses of the diodes in the half-cycle are equal to:

$$\begin{aligned} P_{loss,D} &= \tfrac{2}{T_s}\left[\int_0^{T_s/2} D(t) i_{L2}(t) V_D dt + \int_0^{T_s/2} (1 - D(t))(i_{L1}(t) - i_{L2}(t)) V_D dt\right] \\ &= \tfrac{2}{Ts}\int_0^{T_s/2} (2D(t)) i_{L2}(t) V_D dt = \tfrac{N V_{in} V_D}{V_o} i_{L1,\max}\left[\tfrac{Ts}{2} - \tfrac{4 V i_n N}{3\omega}\right], \end{aligned} \tag{37}$$

and the losses due to switching on and off the diodes are equal to:

$$p_{rr} = 2 n f_s Q_{rr} \frac{V_o}{n} = 2 f_s Q_{rr} V_o, \tag{38}$$

where Q_{rr} is the recovery charge of each diode that is determined by the diode datasheet.

4. Control Strategy

In the proposed converter, the hysteresis method is used for controlling the circuit. Hysteresis current control is a suitable switching method used in all types of structures for managing the current of power converters due to its simplicity, high stability, fast dynamic behaviour, and high accuracy. According to the performance of the circuit, when the S_1 switch is on in positive half-cycle (S_2 switch is on at negative half cycle) and the S_3 switch is off (S_4 switch is off) in Figure 3, the L_1 inductor is charged and its current increases, and when the S_3 switch on the positive half-cycle is on (S_4 switch on the negative half cycle is on) and the S_1 switch is off (S_2 switch is off) in Figure 4, the L_1 inductor is discharged and its current decreases. The principle of the hysteresis method in this converter is that a single-phase sinusoidal reference wave is compared with the input voltage (reference current) with the inverted L_1 current. A hysteresis bandwidth is considered to be limited between the upper and lower band. The performance of the converter in negative and positive half-cycles is as follows.

First mode in the positive half-cycle: reference current is evaluated with inductor current L_1. If the L_1 inductor current reaches the upper hysteresis band, the S_3 switch turns on and the S_1 switch turns off, and the L_1 inductor current decreases, and if the input current L_1 reaches the lower hysteresis band, the S_1 switch turns on and the S_3 switch turns on. It turns off and this process continues until it enters the negative half cycle.

The second mode in the negative half-cycle: this mode is similar to the previous mode and the reference current is compared with the input current of L_1. If the L_1 inductor current reaches the upper band, the S_2 switch will turn on and the S_4 switch will turn off. Also, if the input current reaches the lower band of the L_1 current, the S_3 switch will turn on and the S_2 switch will turn off.

If the hysteresis bandwidth is high, the switching frequency will decrease and the THD of the current source will increase. If the hysteresis bandwidth is low, the switching

frequency will increase and, as the switching speed increases, the accuracy of the reference current will increase, and the THD of the current source will decrease; however, the problems caused by the increase in the switching frequency will increase.

The disadvantage of the hysteresis method is that the switching frequency varies, which causes noise and increases the switching loss, and injects high-frequency current components into the current source.

5. Converter Validation

5.1. Simulation Results

A converter with a three-stage CW multiplier has been designed and simulated to assess the performance of the proposed converter. The size of the circuit elements is considered in Table 2 according to the values obtained from the theoretical results.

Table 2. Main parameters of converter prototype.

Symbols	Definitions	Values
$V_{in\ (rms)}$	Input voltage	220 V
$V_{out\ (DC)}$	Output voltage	1200 V
P_{out}	Output power	1000 W
L_1	Inductance	2.8 mH
L_2	Inductance	9.7 mH
C	CW capacitance	470 µH
R	Output resistance	1440 Ω
f_s	Maximum switching frequency	150 kHz
f_n	Line frequency	60 Hz
V_D	Diode forward voltage	0.95 V
D	Duty cycle	-

The simulation results of the converter are provided with the CW multiplier of one level; the value of the reference current is given to the converter with the desired line frequency and amplitude. Converter switching is aimed at tracking the input current of the converter. In this simulation, the multiplier of one level and the values of the convertor elements are simulated according to the values calculated in the previous section.

Figure 8 represents the implemented control scheme for the proposed converter in simulation and experimental results. We sample the input voltage and use it to determine the phase of reference current as of the input voltage and the input current should be in phase for PFC operation. The microcontroller determines the magnitude of the reference current waveform according to the required output voltage. The switching commands for S_1 to S_4 are generated by the microcontroller. Since the switching commands are generated by a current hysteresis algorithm, the switching frequency is not constant. Selecting a narrow hysteresis bandwidth reduces the THD value but increases the switching losses. Therefore, there is a tradeoff between output power quality and converter efficiency. The instantaneous value of the reference current is obtained by sampling the input voltage (to provide a power factor correction operating condition). In order to change the input current value, the reference current must be changed through the microcontroller. The hysteresis band for the experimental setup is adjusted to 0.2 Volts. The switching frequency is not constant but has an average value of 150 kHz. Figure 9 compares input current THD for two different current controls: (1) close-loop simple current control and (2) hysteresis current control. The input current THD was calculated to be 4.93% and 1.22% for the closed-loop control and hysteresis current control, respectively.

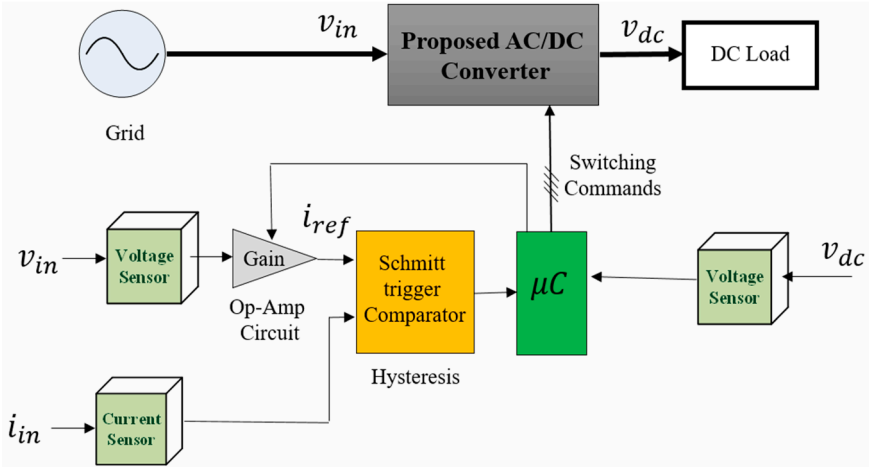


Figure 8. The implemented control scheme for the proposed converter.

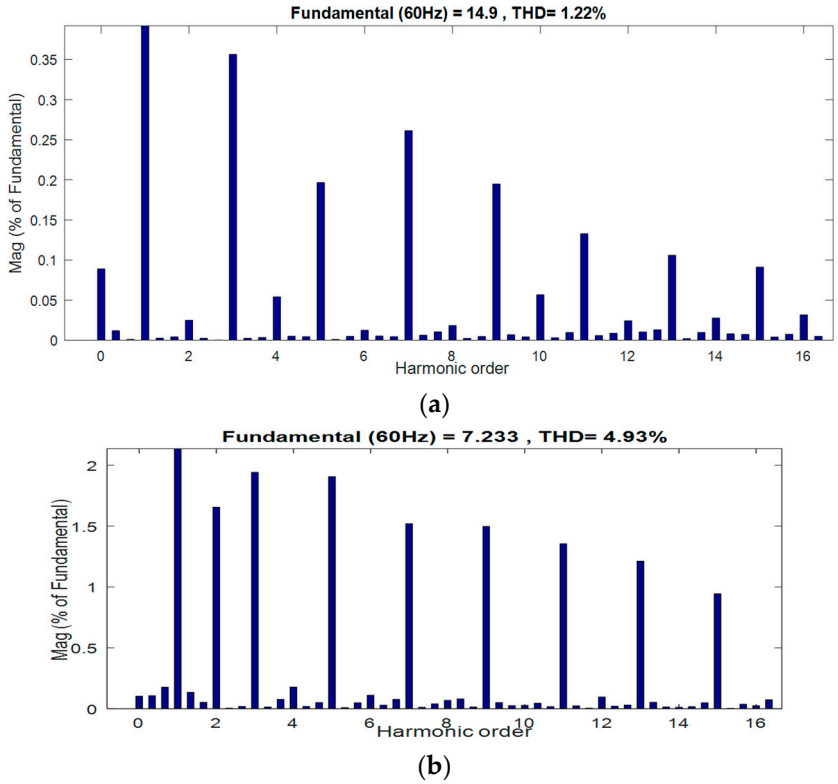


Figure 9. THD value for the input current of the converter: (**a**) closed loop simple current control, (**b**) hysteresis current control.

Figure 10a shows the amount of reference current with an amplitude of 15 A and Figure 10b shows the converter input current that the reference current follows, and as can be seen, the input current is sinusoidal. In Figure 11, the waveform of the converter output voltage is shown, and the output voltage of the converter is shown in Figure 9b. In Figure 12, the shape of the input voltage and input currents is shown simultaneously. As can be seen, the input voltage and input current are all-phase. The current of the L_2 inductor is shown in Figure 13. As can be seen, due to the use of the hysteresis control method, the L_2 inductor current is almost sinusoidal. The THD of the input current in this method is 1.22%, as shown in Figure 14.

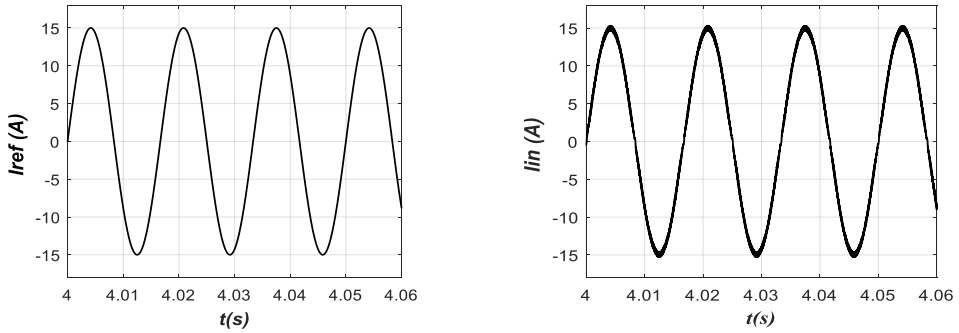


Figure 10. Waveforms of the converter provided by the hysteresis control method: (**a**) reference current, (**b**) input current.

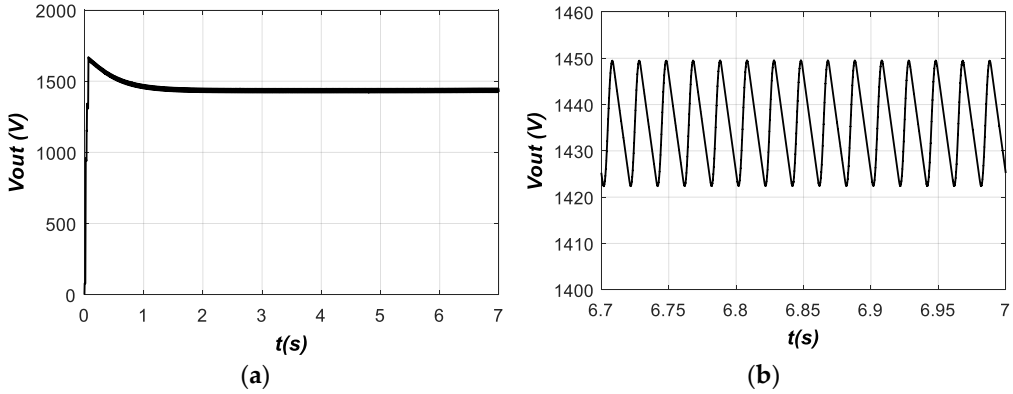


Figure 11. (**a**) output voltage waveform with (**b**) extended output voltage.

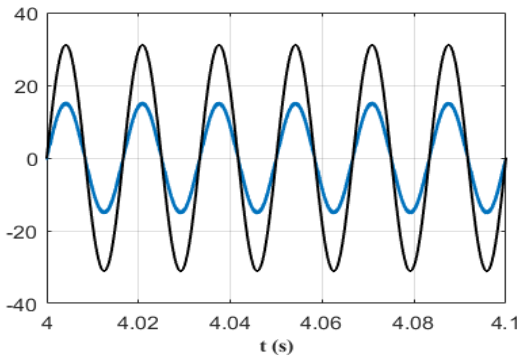


Figure 12. Voltage waveform and input current provided by the converter.

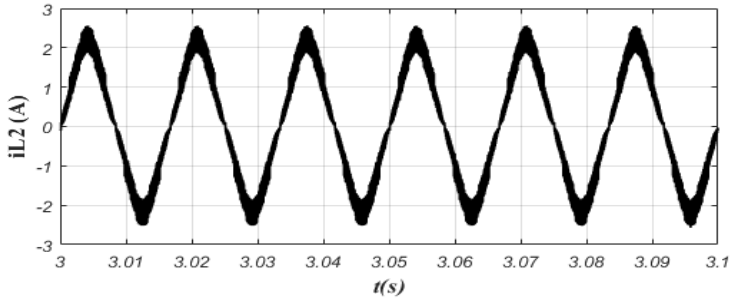


Figure 13. L_2 inductor current in hysteresis method.

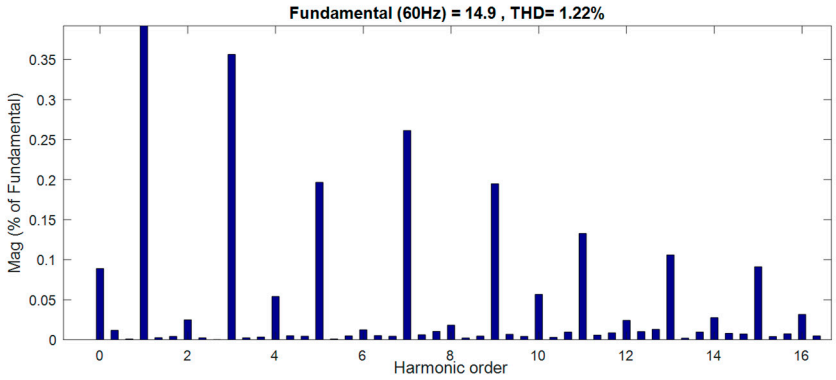
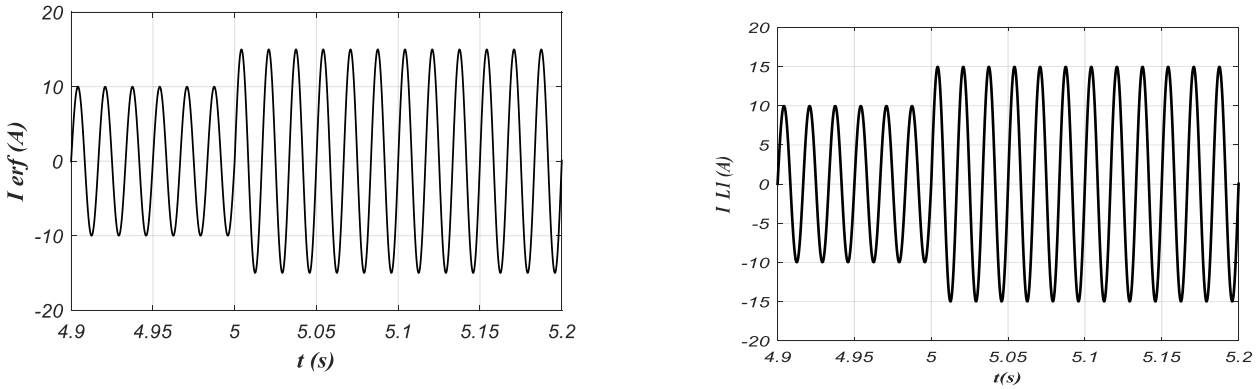


Figure 14. THD diagram of the input current in the hysteresis method.

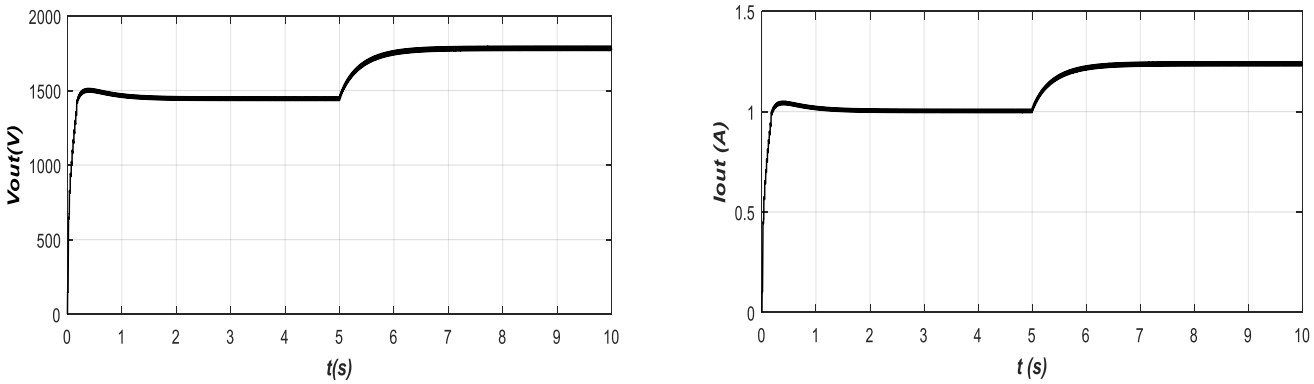
In Figure 15a, the amplitude of the reference current changes from 10 A to 15 A after 5 s. As can be seen from Figure 15b, the value of the converter input current has also changed from 10 A to 15 A after 5 s.



(**a**) (**b**)

Figure 15. The waveform of the input current in the hysteresis method: (**a**) reference current, (**b**) converter input current.

The output voltage waveform is shown in Figure 16a, and the output current waveform is shown in Figure 16b; as expected, the value of current and voltage changes after 5 s and converge to new values.



(**a**) (**b**)

Figure 16. (**a**) The output voltage waveform and (**b**) the output current waveform for the converter.

Figures 10 and 12 demonstrate that the converter is able to provide power factor correction in the AC side and track the reference current waveform with a neglected error.

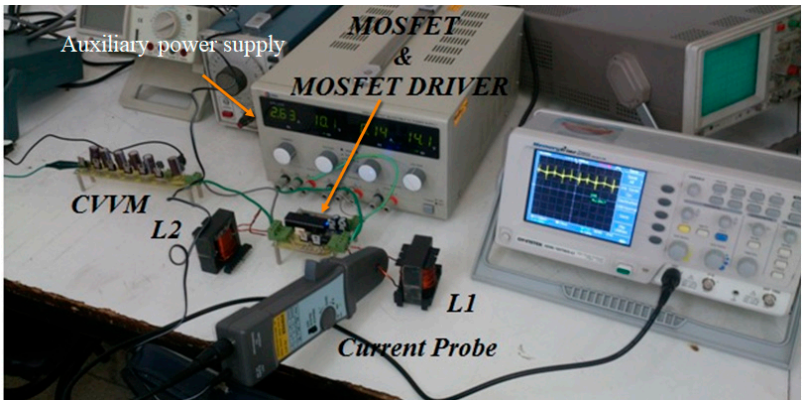
THD is also accepted as shown by Figure 14. For the output voltage, the ripple has good consistency with theoretical predictions (Figure 11).

5.2. Experimental Results

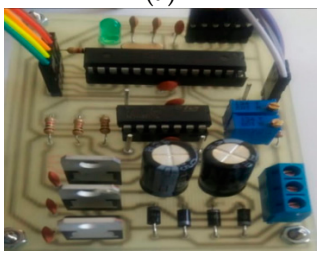
A converter with specifications listed in Table 3 is provided for experimental validation of the theoretical part. This converter uses the hysteresis controller and the three-level multiplier. The prototype is shown in Figure 17.

Table 3. Converter prototype parameters.

Components	Type
L_1 inductor	0.5 mH
L_1 resistance	0.3 Ω
L_2 inductor	9.7 mH
L_2 resistance	0.25 Ω
Three-level multiplier capacitors	470 µF Electrolytic
Three-level parallel multiplier capacitors	100 nF MKT
Three-level multiplier diodes	Fast Diode UF5408
Diode forward voltage	0.6 V
Power switches	MOSFET IRF840
Switch conduction resistance	0.07 Ω
Switch gate driver	TLP250
Current sensor	ACS712ELCTR-20A-T
Input current reference	I_{PK} = 2 A
Converter input voltage	Vin = 5 V_{RMS}
Input voltage (RMS)	220 Volts
Input voltage frequency	50 Hz
Output rated power	1 kW
Output load	3 kΩ



(**a**)



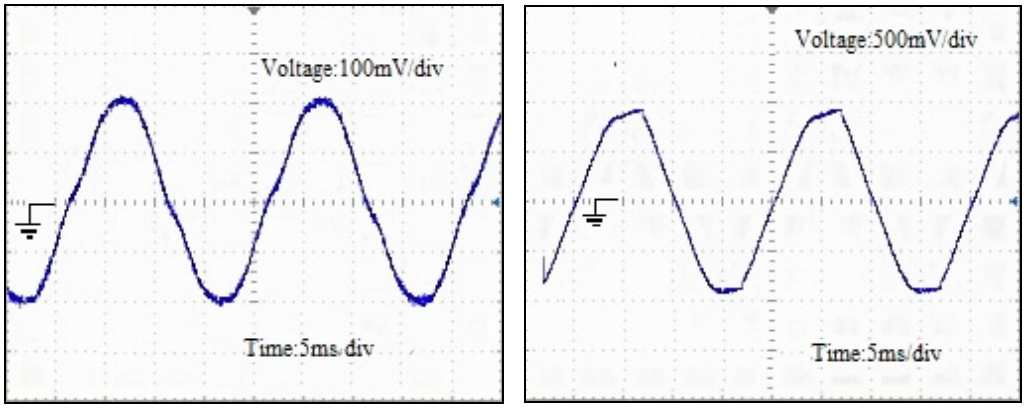
(**b**)

Figure 17. Prototype of the proposed converter: (**a**) experimental setup, (**b**) control and sampling circuit of the converter.

The built-in converter has three parts. The first part is related to the CW voltage multiplier circuit and converter and load inductors, and the second part is related to the

converter control section. The input voltage is applied to the microcontroller using a step-down transformer 220/9 V, resistive division, and op-amp circuits to the appropriate voltage level in order to generate the reference current and then the reference is entered into the microcontroller. The third part is related to converter switches with gate drives, which have separate sources due to the isolation of voltages related to gate drives. A heat sink has been used to increase the temperature of the switches.

The waveform of the reference current is shown in Figure 18a. The microcontroller determined the required current magnitude according to the feedback from the output voltage. As shown, in order to provide a 115 V in the output, it is required to inject a peak value of 4 A into the converter. This waveform is compared to the input current through the current sensor, and the appropriate switching commands are generated for the switches. The input current of the converter is shown in Figure 18b.



(**a**) (**b**)

Figure 18. (**a**) Input current measured by sensor (1A/div), (**b**) input reference current (1000 mV/div).

The reference current has the same phase as the input voltage because it is obtained by using a resistive division and only 2 V and above are given turns. The waveform of the input current and the reference current is shown in Figure 19. As can be seen, both are homogeneous. The upper waveform of Figure 19 is related to the reference current, and the lower waveform is related to the input current measured by the flow sensor.

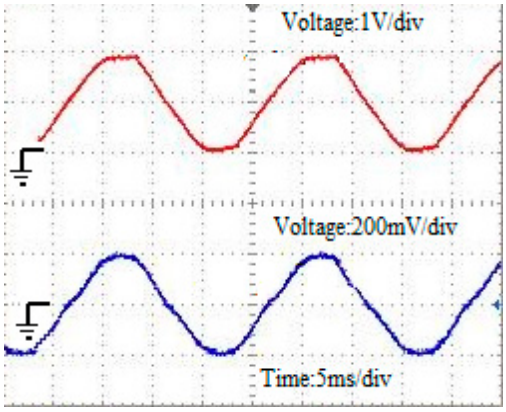


Figure 19. Input voltage waveform and the reference current (2V/div, 2A/div).

Considering all the practical limitations, the input current of the converter is shown in Figure 19 (experimental result) and Figure 20 (simulation result). The voltage waveforms of the capacitors of the voltage multiplier circuit are shown in Figure 21. The capacitor voltage C_1 is half the voltage of the other capacitors, as expected. The voltages of capacitors C_2, C_4, and C_6 are reduced compared to capacitors C_3 and C_5 due to the fact that they provide output current which is shown in Figure 22.

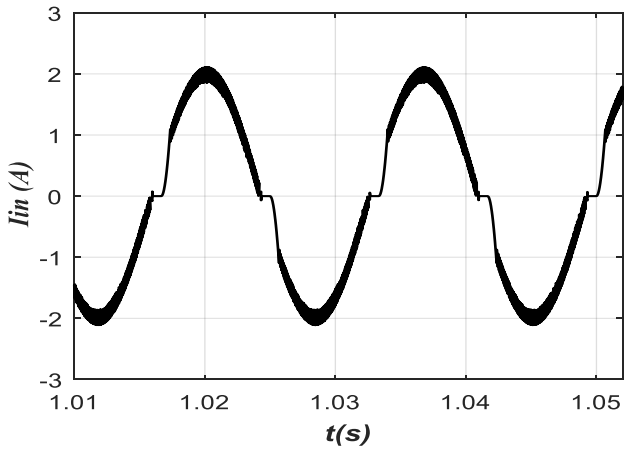


Figure 20. Simulation result for input current waveform of L_1 inductor.

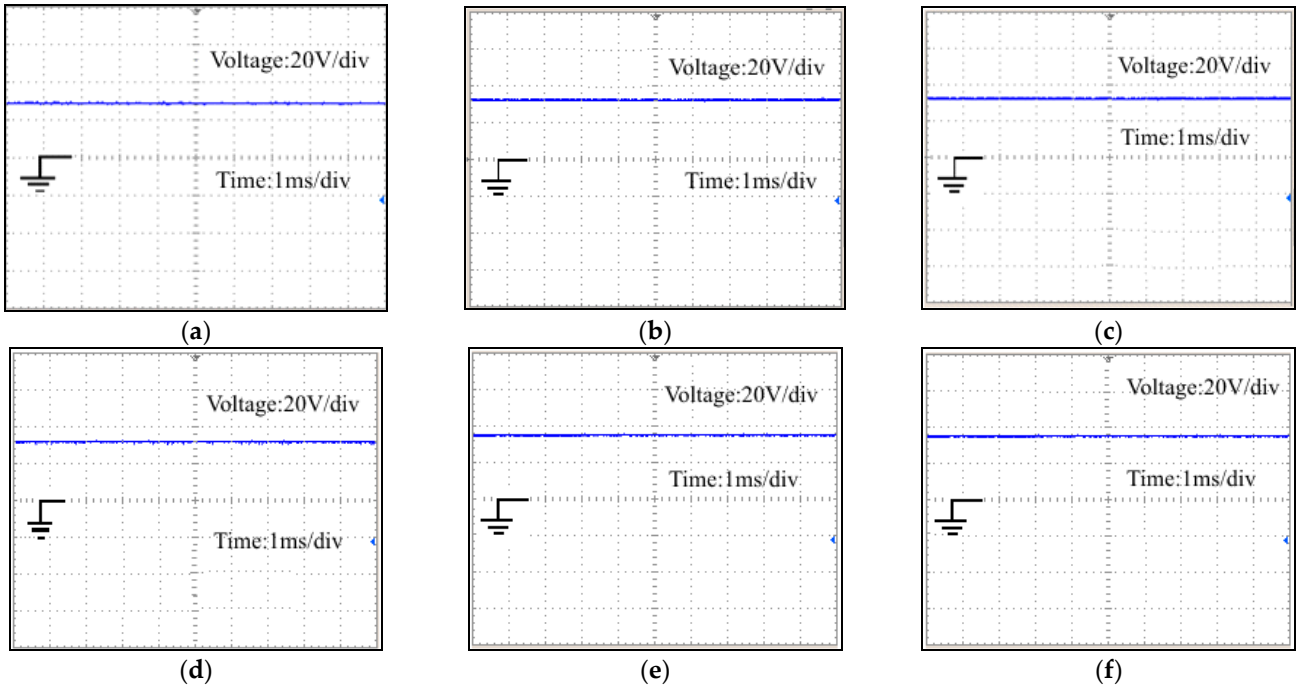


Figure 21. CW voltage multiplier waveforms in experimental mode (20 V/div): (**a**) Capacitor C_1, (**b**) Capacitor C_2, (**c**) Capacitor C_3, (**d**) Capacitor C_4, (**e**) Capacitor C_5, and (**f**) Capacitor C_6.

The waveform of the transient and steady-state of the output voltage is shown in Figure 23a and the simulation state is shown in Figure 23b.

The input voltage of the converter is shown in Figure 24, which can be seen as the effective value of which is 5 V.

Finally, in order to obtain a better assessment for the power loss of the converter, converter power loss versus the output power, and also efficiency diagram based on the variation of output power, the overall losses based on the variation in output power are compared in Figure 25.

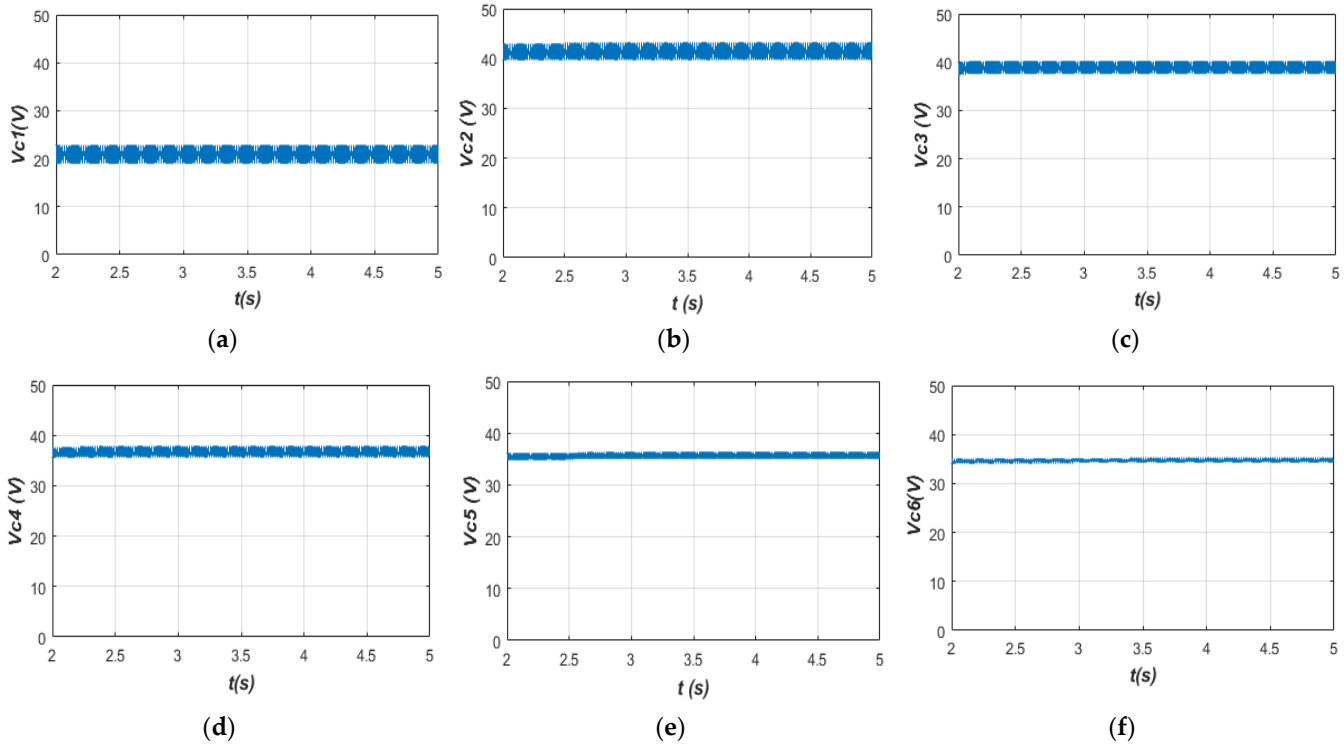


Figure 22. CW voltage multiplier waveforms in simulation mode: (**a**) Capacitor C_1, (**b**) Capacitor C_2, (**c**) Capacitor C_3, (**d**) Capacitor C_4, (**e**) Capacitor C_5, and (**f**) Capacitor C_6.

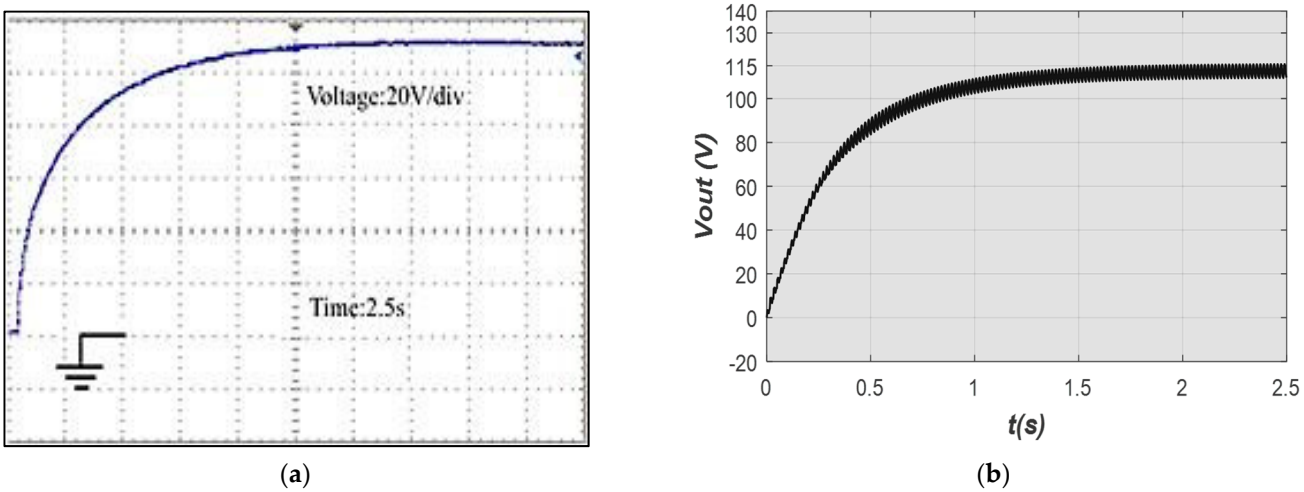


Figure 23. (**a**)The output waveform of the converter voltage in experimental mode (20 V/div); (**b**) in simulation mode.

5.3. Comparison between the Proposed Converter and State-of-the-Art Rectifiers

Comparison between the proposed converter and state-of-the-art rectifiers in terms of voltage gain, voltage stress of components, and number of switches are presented in Table 4. The proposed converter voltage gain is higher than [45]. Also, ref. [46] shows a marginally higher voltage gain but the number of elements is higher, particularly in a higher number of stages. The number of elements for the proposed converter is lower than [47] while the other characteristics are the same.

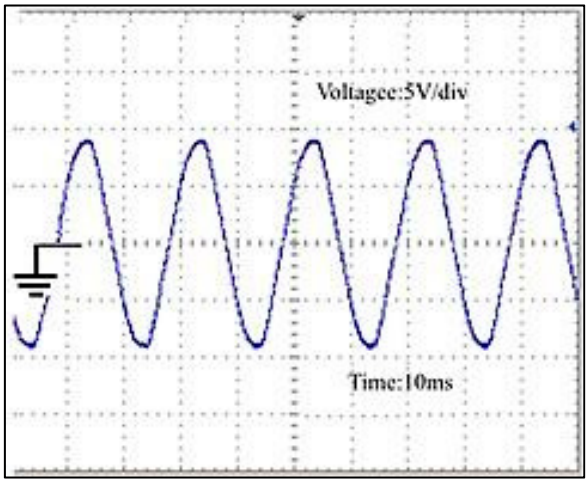
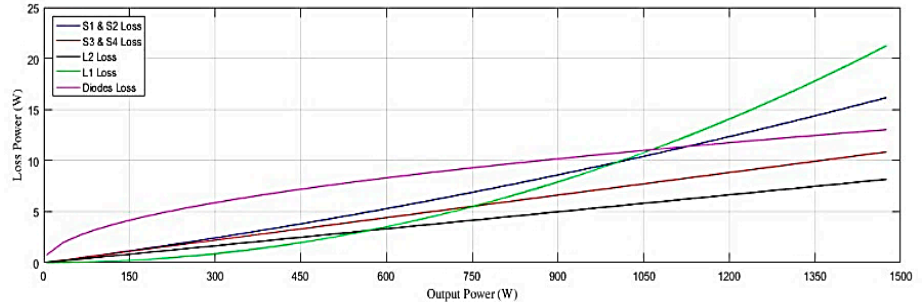
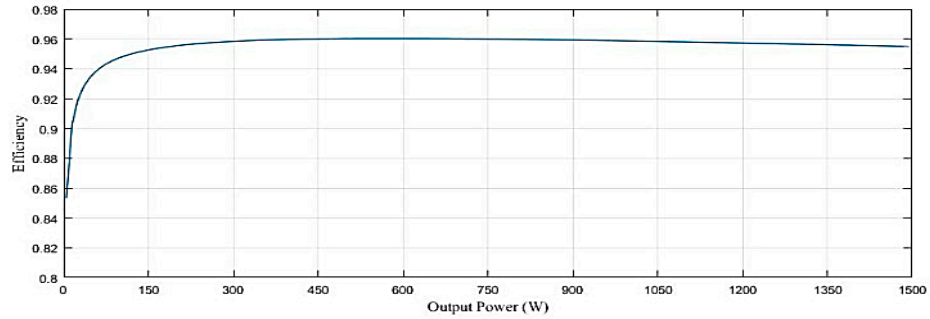


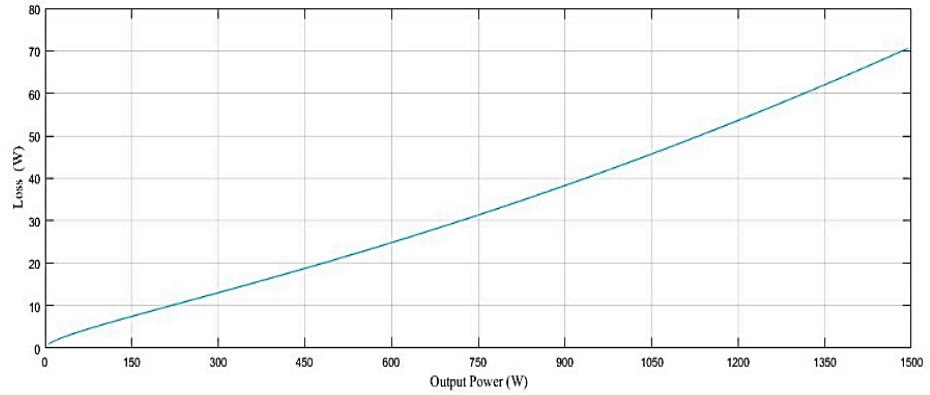
Figure 24. The input voltage of the converter (5 V/div).



(**a**)



(**b**)



(**c**)

Figure 25. Power loss analysis of the proposed converter, (**a**) different parts of the converter power loss, (**b**) the converter loss, (**c**) efficiency.

Table 4. Comparison between the proposed converter and state-of-the-art rectifiers.

	Proposed Converter	**[47]**	**[46]**	**[45]**
Gain	$\frac{2n}{1-D}$	$\frac{2n}{1-D}$	$\frac{2n+1}{1-D}$	$\frac{1}{1-D}$
Capacitors voltage stress	$\begin{cases} \frac{V_o}{n} & k=1 \\ \frac{V_o}{2n} & k\neq 1 \end{cases}$	$\begin{cases} \frac{V_o}{n} & k=1 \\ \frac{V_o}{2n} & k\neq 1 \end{cases}$	$\frac{V_o}{2n}$	V_o
Number of elements	$6+4\,n$	$9+4\,n$	$5+6\,n$	8
Switches voltage stress	$\frac{V_o}{2n}$	$\frac{V_o}{2n}$	$\frac{V_o}{2n}$	V_o
Diodes voltage stress	$\frac{V_o}{2n}$	$\frac{V_o}{2n}$	$\frac{V_o}{2n}$	V_o
Number of switches	4	8	4	1

6. Conclusions

In this paper, a new topology of AC/DC converter using a high-voltage CW multiplier structure is presented. The main benefit of the converter is providing high voltage gain and the ability to work in PFC conditions. Moreover, the CCM circuit operation, design considerations, operating range, and loss calculations were investigated. Experimental results are consistent with the theoretical analyses carried out throughout this paper. Also, a comparison between this converter and several other converters was demonstrated in order to evaluate the proposed topology with other methods. This converter has relatively few elements as well as a high output voltage and low stresses compared to other works. The output voltage of the converter was adjusted to 115 V and the voltage ripple was lower than 2%. The input current THD were calculated as 4.93% and 1.22% for the closed-loop control and hysteresis current control, respectively. Due to the increasing DC loads on the power system, it can be concluded that this converter can be used on a large scale in the power grid as well as for sustainable renewable energy which employs AC generators such as wind energy systems. Therefore, improving the performance of the converter and reducing losses as well as its implementation and construction must be considered.

Author Contributions: Investigation, A.Z. and A.R.; methodology, A.Z., M.S. and A.R.; supervision, A.R.; software, A.Z. and A.R.; validation, A.Z. and A.R.; writing—original draft preparation, A.Z. and H.M.-M.; writing—review and editing, A.R. and M.S. All authors have read and agreed to the published version of the manuscript.

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