Switching Strategy Development, Dynamic Model, and Small Signal Analysis of Current-Fed Cockcroft-Walton Voltage Multiplier

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ABSTRACT High voltage generation, is one of the main applications of the Cockcroft-Walton voltage multiplier (CWVM), however recently this structure is investigated to be used for high step-up DC-DC applications. This paper discusses dynamic behaviour and small-signal modelling of a CWVM based DC-DC converter and investigates how switching strategy can affect the dynamic performance of the converter. This study firstly presents, a new switching method, the steady-state relations are derived and compared to the conventional switching strategy, which shows that the proposed method equilibrates the voltage and current stress of the switches and decreases the current ripple of the input inductor. Then, the converter is dynamically modelled and analyzed using the pole-zero map. The analysis shows that the proposed switching strategy improves the dynamic behaviour of the converter. The effect of the passive elements on dynamic performance is also discussed. Experimental results are presented for a 160 W prototype to validate the evaluated performance and the dynamic analysis.

INDEX TERMS DC-DC power converters, modeling, pulse width modulation, photovoltaic systems, switching converters, voltage control.

I. INTRODUCTION

Since fossil fuels had massive impacts on environmental pollution over the past decade, there has been significant attention to renewable energy sources, such as wind, photovoltaic (PV), fuel cells. PV systems have been considered as an attractive choice [1] because of sustainability and availability, but one of the main challenges is the limited and variable output voltage of PV panels [2]. Typically the voltage of a maximum power point (MPP) in a single PV panel is lower than 50 V [3]. This makes it inevitable to use a power processing system to step up the voltage. A simple solution is a series connection of the PV panels to increase the output voltage, but it declines the MPP efficiency in case of any disturbance such as shading, different orientation of PV panels, pollution, different panel manufacturers, and unequal ageing [4]. The second solution is stepping up the voltage using a boost converter (Fig. 1). To make use of this kind of source commercially viable, a simple, low-cost and high-efficiency power conversion topology should be developed. Various topologies have been developed to introduce high step-up converters without an extremely high duty ratio, which are reviewed in [5]. Generally, they are categorized based on which element has an important role in voltage boosting:

- Transformer and coupled inductor [6]
- Impedance network [7], [8].
- Switched inductor/capacitor [9].

In the last decades, several topologies of switched capacitor voltage multiplier or charge pump circuits have
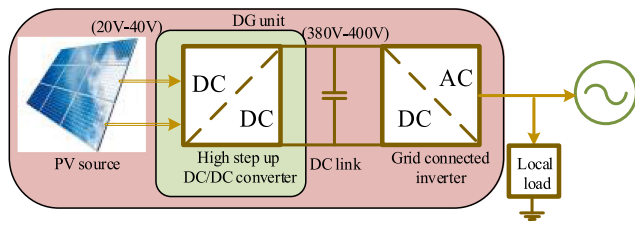
FIGURE 1. Schematic of an n-stage CWVM with AC input voltage.
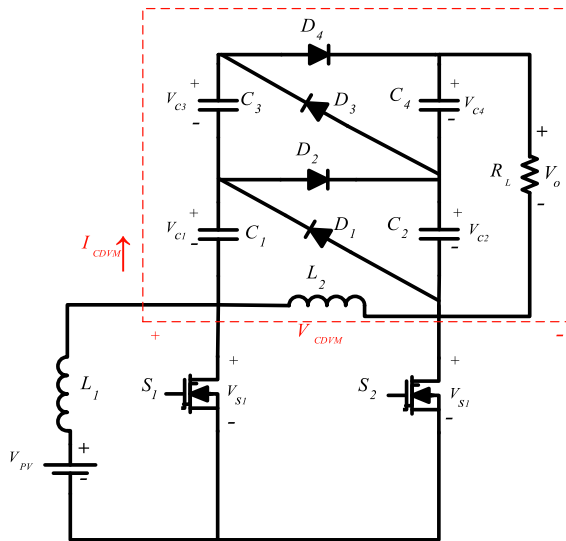

FIGURE 2. Circuit configuration of the dual inductor dual switch current-fed Cockcroft-Walton Voltage Multiplier using n-stage CWVM.

been developed including Marx generator, Cockcroft–Walton voltage multiplier (CWVM) (also known as Greinacher multiplier and Villard cascade), Falkner, Cernea, Dickson, etc [10]–[13]. Hybrid topologies are also introduced such as Falkner-Dickson parallel voltage multiplier [14], and Cockcroft–Walton/Dickson Multiplier [15]. These topologies are used in many applications such as chip design, energy harvesting, and high voltage generations. Marx generator and CWVM are the main structures used for high voltage DC applications [10], [16] such as X-ray equipment, neutron radiography [17], plasma generator [18], particle acceleration [19], and radar systems.

Although conventional low-frequency CWVM (Fig. 1) has been widely used for high voltage DC generators, employing a power electronic interface to provide high-frequency AC voltage at the input of CWVM provides several advantages such as faster response, better controllability, smaller passive elements, and lower output ripple [20]–[22]. CWVM is categorized into two types; voltage-fed and current-fed, which current-fed shows higher voltage gain and reliability. One of the recently introduced topologies employing a current-fed CWVM connected to a current boost converter is shown in Fig. 2 [19]. The main advantages of the current-fed converters are high voltage step-up capability, low voltage stress and soft switching on the semiconductor devices, improved efficiency,

continuous input current suppressing the start-up inrush current.

One of the main constraints of CWVM circuits is the limited output voltage regulation. It is because of the series connection of capacitors [20]. Therefore, transient analysis of the output voltage particularly during load variation is necessary. To achieve this, deriving the dynamic model and analysing the converter behaviour is necessary. In [21], a time-variant dynamic model for a current-fed CWVM is presented, which can be used for transient simulation but is not suitable for deriving transfer functions and plotting pole-zero map and bode diagrams.

In this paper, the dynamic behaviour of the CWVM-based converter shown in Fig. 2 is discussed. In Section II, A new switching strategy based on the overlap time control of the switches is proposed and the steady-state operation using this strategy is described. Compared to the conventional method, it improves the voltage gain and balances the voltage stress and the conduction losses of the switches. In Section III, the dynamic large-signal and small-signal models of the converter are obtained and input-to-output (G_{vg}) and control-to-output (G_{vd}) transfer functions are derived. Using these relations, the pole-zero maps are plotted and the transient behaviour of the converter is discussed. To verify the performance of the proposed converter, a 160 W laboratory prototype is implemented which the results are shown in Section IV. The results validate the theoretical analysis and the practicability of the presented high step-up voltage multiplier circuit.

The main contributions of this paper are as follows:
1) Proposing a new switching strategy to improve the steady-state and dynamic characteristics of the current-fed CWVM converter. The main merits of the proposed switching method are as follows:
   - Balancing the voltage stress and power loss of the power switches, which improves the thermal management of the converter.
   - Reducing the ripple of the input current.
   - Higher voltage gain compared to the conventional switching method.
   - Comparing the pole-zero maps showed, the RHP zeros are farther from the origin (compared to the conventional strategy).
2) Efficiency and steady-state analysis of the converter.
3) Dynamic modelling of the converter and analysis of the dynamic performance of the converter.
4) Exploring the experimental results.

II. OVERLAP TIME CONTROL SWITCHING STRATEGY AND STEADY-STATE OPERATION PRINCIPLES OF THE CONVERTER

Operation principles for complementary switching of the switches called here as conventional switching strategy is described in [19]. In this section, a new switching strategy based on the overlap time intervals of the switching commands is presented and the steady-state relations are derived.
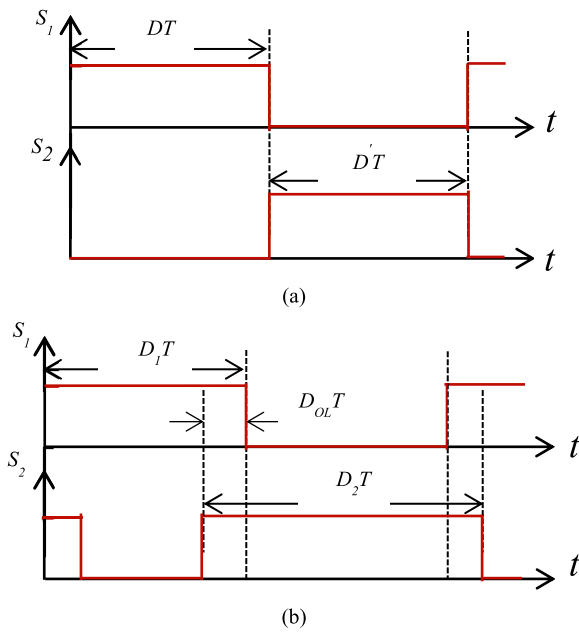
FIGURE 3. The converter switching commands, (a) conventional and (b) proposed strategy.

FIGURE 4. Current paths for the different operation States of the converter, (a) state I, (b) state II, and (c) State III.

The converter is assumed to be ideal and work in continuous conduction mode (CCM).

In Fig. 3, the commands in a switching period (T) for the conventional and the presented methods are shown. In the conventional method (Fig. 3(a)), S_1 switches with a certain duty cycle (D) and the state of S_2 is logically NOT of S_1, while a small overlap duration is practically necessary to guarantee the current path of I_{L1}. In the presented switching strategy (Fig. 3(b)), the commands for S_1 and S_2 have PWM waveforms with D_1 and D_2 duty ratios respectively, while a time shift equals to $T/2$ is considered. Although D_1 and D_2 could generally have different values, the following condition should be always satisfied; $D_{OL} > 0 \rightarrow D_1 + D_2 > 1$.

Considering the presented switching method, the converter contains three states in CCM that in states I and II, have 2 sections, as described in the following. The current paths during the three states are shown in Fig. 4 and the main current and voltage waveforms are illustrated in Fig. 5.

State I: S_1 is on, and S_2 is off. This state lasts for $(1 - D_2)T$ and the current paths are shown in Fig. 4(a). L_1 is charged through the input voltage source and L_2 feeds the multiplier circuit, therefore it is discharged. Relations are derived by calculating currents passing through the diodes in two sections. In each section, only one diode is on, and the diodes are turned on and off according to key waveforms of Fig. 5.

Section I: in this section, diode D_3 is on and diode D_1 is off. The relations of the inductors voltages and the capacitor currents are as follows:

$$v_{L1} = V_{IN} \tag{1}$$
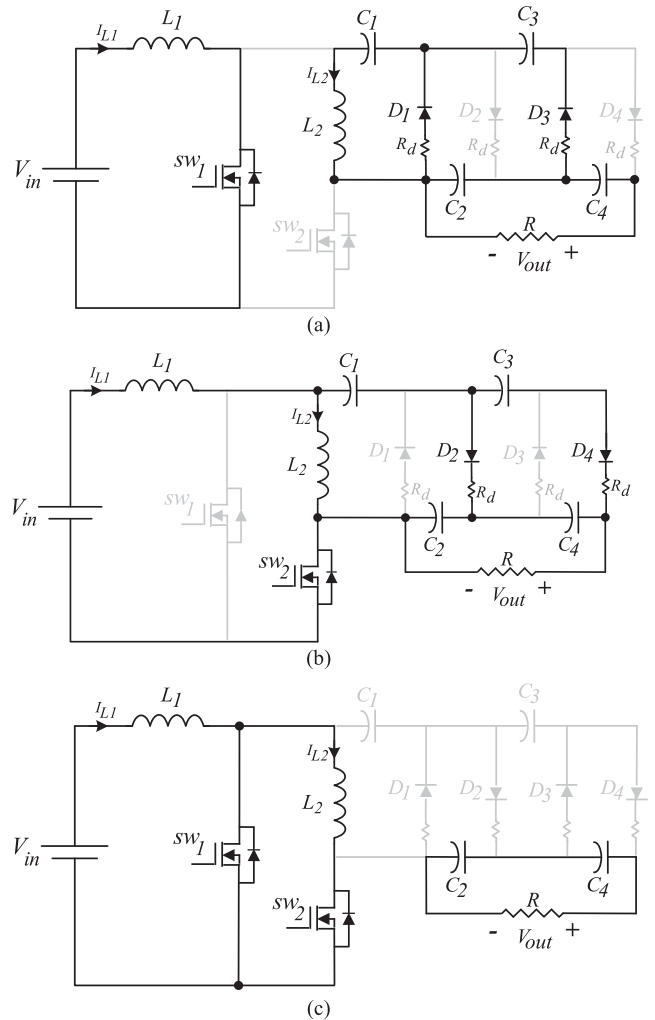
$$v_{L2} = V_{C2} - V_{C3} - V_{C1} - I_{L2}R_d \tag{2}$$

$$i_{c1} = i_{L2} \tag{3}$$

$$i_{C2} = -\frac{V_{C2} + V_{C4}}{R} - I_{L2} \tag{4}$$

$$i_{C3} = I_{L2} \tag{5}$$

$$i_{C4} = -\frac{V_{C2} + V_{C4}}{R} \tag{6}$$
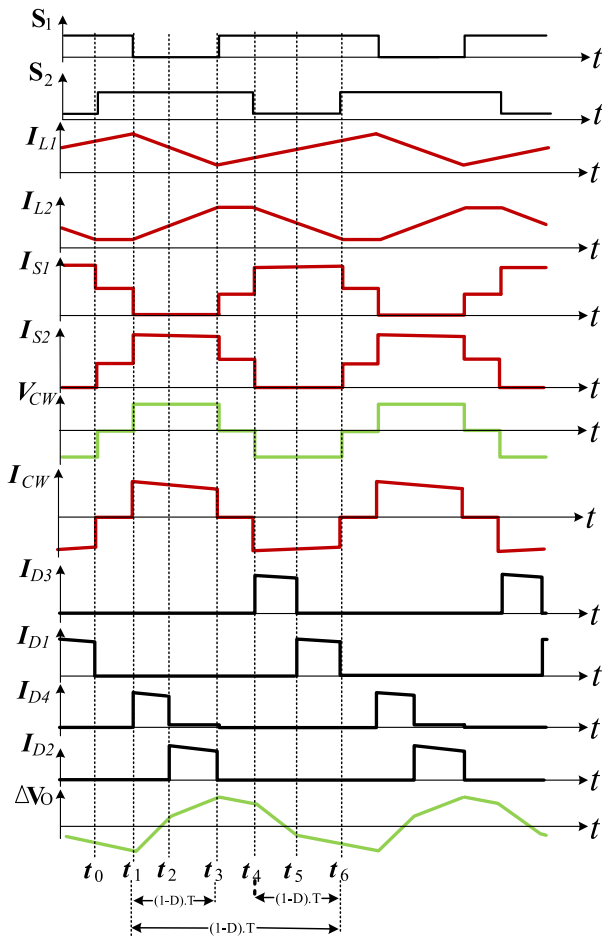
where R_d denotes diode resistance.

Section II: in this section, the condition is the same as Section I except, diode D_1 is on and diode D_3 is off. The relations are as follows:

$$v_{L1} = V_{IN} \tag{7}$$

$$v_{L2} = -V_{C1} - I_{L2}R_d \tag{8}$$

$$i_{C1} = i_{L2} \tag{9}$$

$$i_{C2} = -\frac{V_{C2} + V_{C4}}{R} \tag{10}$$

FIGURE 5. Key waveforms of the power converter with the proposed switching strategy.

$$i_{C3} = 0 \tag{11}$$

$$i_{C4} = -\frac{V_{C2} + V_{C4}}{R} \tag{12}$$

State II: S_1 is off, and S_2 is on. This state lasts for $(1 - D_1)T$ and the current paths are shown in Fig. 4(b). Energy stored in L_1 is delivered to L_2 and CWVM circuit. Therefore, L_1 and L_2 are discharged and charged respectively. Like state I, there are two sections.

Section I: in this section based on Fig. 4, diode D_4 is on and diode D_2 is off. The relations for the inductor voltages and the capacitor currents are as follows:

$$v_{L1} = V_{IN} + V_{C1} + V_{C3} - V_{C2} - V_{C4} - (I_{L1} - I_{L2})R_d \tag{13}$$

$$v_{L2} = -V_{C1} - V_{C3} + V_{C2} + V_{C4} + (I_{L1} - I_{L2})R_d \tag{14}$$

$$i_{C1} = -I_{L1} + I_{L2} \tag{15}$$

$$i_{C2} = I_{L1} - I_{L2} - \frac{V_{C2} + V_{C4}}{R} \tag{16}$$

$$i_{C3} = -I_{L1} + I_{L2} \tag{17}$$

$$i_{C4} = I_{L1} - I_{L2} - \frac{V_{C2} + V_{C4}}{R} \tag{18}$$

Section II: the condition in this section is the same as Section I except that diode D_2 is on and diode D_4 is off. The relations are as follows:

$$v_{L1} = V_{IN} + V_{C1} - V_{C2} - (I_{L1} - I_{L2})R_d \tag{19}$$

$$v_{L2} = -V_{C1} + V_{C2} + (I_{L1} - I_{L2})R_d \tag{20}$$

$$i_{C1} = -I_{L1} + I_{L2} \tag{21}$$

$$i_{C2} = I_{L1} - I_{L2} - \frac{V_{C2} + V_{C4}}{R} \tag{22}$$

$$i_{C3} = 0 \tag{23}$$

$$i_{C4} = -\frac{V_{C2} + V_{C4}}{R} \tag{24}$$

State III: Both switches are on. This state lasts for $(D_1 + D_2 - 1)T$ and the current paths are shown in Fig. 4(c). L_1 is connected to the input, therefore, it is charged, L_2 is shorted and its current remained constant during this state. No current is injected into the CWVM circuit and the output capacitors provide the load current. The relations are as follows;

$$v_{L1} = V_{in} \tag{25}$$

$$v_{L2} = 0 \tag{26}$$

$$i_{C1} = 0 \tag{27}$$

$$i_{C2} = -\frac{V_{C2} + V_{C4}}{R} \tag{28}$$

$$i_{C3} = 0 \tag{29}$$

$$i_{C4} = -\frac{V_{C2} + V_{C4}}{R} \tag{30}$$

Considering the converter circuit in different states, the main waveforms of the converter are extracted which are shown in Fig 5. V_{SW}, I_{SW}, and ΔV_o are the switch voltage and current, and the output voltage ripple respectively. V_{cw} and I_{cw} are the voltage and current of the capacitor.

Applying the inductor volt-second and capacitor charge balances and assuming $R_d = 0$ yield the steady-state relations for the capacitor voltages and inductor currents;

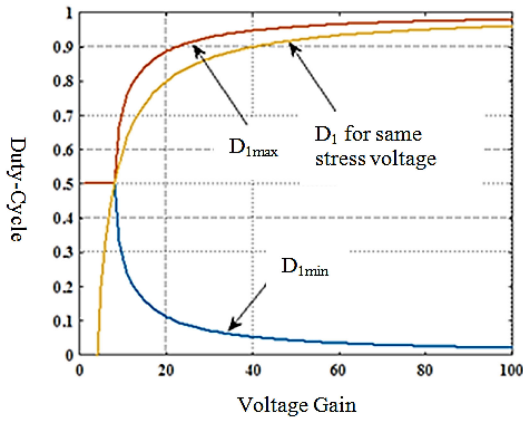$$I_{L1} = \frac{4V_{in}(D_1' + D_2')^2}{R D_1'^2 D_2'^2} \tag{31}$$

$$I_{L2} = \frac{4V_{in}(D_1' + D_2')^2}{R D_1' D_2'^2} \tag{32}$$

$$V_{C1} = \frac{V_{in}}{D_2'} \tag{33}$$

$$V_{C2} = V_{C3} = V_{C4} = \frac{(D_1' + D_2')}{D_1' D_2'} V_{in} \tag{34}$$

$$V_{out} = V_{C2} + V_{C4} = 2\frac{(D_1' + D_2')}{D_1' D_2'} V_{in} \tag{35}$$

where, $D_1' = (1 - D_1)$ and $D_2' = (1 - D_2)$.

FIGURE 6. D_1 versus voltage gain considering the same voltage stress on the switches.

The converter voltage gain (G) can be obtained as follows;

$$G = \frac{V_{out}}{V_{in}} = 2\frac{(D_1' + D_2')}{D_1' D_2'} \tag{36}$$

Generally, D_1 and D_2 may have different values for a given voltage gain (G). In other words, D_2 can be defined according to G and D_1 as in the following;

$$D_2 = 1 - \frac{2D_1'}{GD_1' - 2} \tag{37}$$

Considering $D_{OL} > 0$, the range of D_1 is theoretically defined by (38) and plotted in Fig. 6.

$$\frac{G - \sqrt{G(G-8)}}{2G} < D_1 < \frac{G + \sqrt{G(G-8)}}{2G} \tag{38}$$

In Fig. 6, D_{1max}, and D_{1min} are the minimum and the maximum values of the duty ratio. Consider that, these limiting values are the value of the duty cycle in the conventional switching strategy [19].

The question is that which value of D_1 is appropriate for a given G. To find the answer, different criteria should be investigated;
- Average values of the inductor currents (I_{L1} and I_{L2}),
- The current ripples (Δi_{L1} and Δi_{L2}).
- The voltage and current stress of the switches.
- The converter power loss and efficiency.

In the following, these criteria are discussed.

A. THE AVERAGE VALUE OF INDUCTOR CURRENTS

I_{L1} and I_{L2} can be written as;

$$I_{L1} = \frac{G^2 V_{in}}{R} \tag{39}$$

$$I_{L2} = \frac{v_{in} G^2 (D_1')}{R} \tag{40}$$

(39) and (40) illustrate that for a given G, I_{L1} is not related to D_1 but I_{L2} decreases for higher D_1; therefore, the higher values of D_1 is more appropriate. This is the main reason that

$0.5 < D < 1$ is practically considered for the conventional switching method.

B. THE CURRENT RIPPLES (ΔI_{L1} AND ΔI_{L2}) AND THE RMS CURRENTS

The other criteria are related to the current ripples, which is calculated as;

$$\Delta i_{L1} = \frac{2D_1' V_{in}}{(GD_1' - 2)L_1 f} \tag{41}$$

$$\Delta i_{L2} = \frac{V_{in}}{L_2 f} \tag{42}$$

(41) and (42) show that D_1 does not affect Δi_{L2} but Δi_{L1} increases with D_1. Therefore, considering $D_1 = D_2$ results in a lower value of Δi_{L1} compared to conventional strategy (D_{1max} in Fig. 6).

The value of RMS current of the inductors according to their waveform is obtained which is equal to [22]:

$$I_{RMS} = i\sqrt{1 + \frac{1}{3}\left(\frac{\Delta i}{I}\right)^2} \tag{43}$$

According to (43) the RMS current of the inductors are equal to:

$$I_{RMS-L1} = \frac{a^2 v_{in}}{R}\sqrt{1 + \frac{1}{3}\left(\frac{\frac{(1-D_2)v_{in}}{Lf}}{\frac{a^2 v_{in}}{R}}\right)^2} \tag{44}$$

$$I_{RMS-L2} = k\sqrt{1 + \frac{1}{3}\left(\frac{\frac{v_{in}}{Lf}}{\frac{a v_{in}(aD_1 - a + 2)}{R(D_1 - 1)}}\right)^2} \tag{45}$$

where $k = \frac{a v_{in}(aD_1 - a + 2)}{R(D_1 - 1)}$. in the same way, the RMS currents of the capacitors are calculated as follows:

$$I_{c1} = \sqrt{I_{RMS-L2}^2 (D_1') + (i_{l2} - i_{l1})_{RMS}^2 (D_2')}$$

$$I_{c2} = \sqrt{S(D_1') + (i_{l1} - i_{l2})_{RMS}^2 (D_2')}$$

$$I_{c3} = \sqrt{\left(\frac{i_{l1}}{2}\right)_{RMS}^2 (D_1') + \left(\frac{i_{l2} - i_{l1}}{2}\right)_{RMS}^2 (D_2')}$$

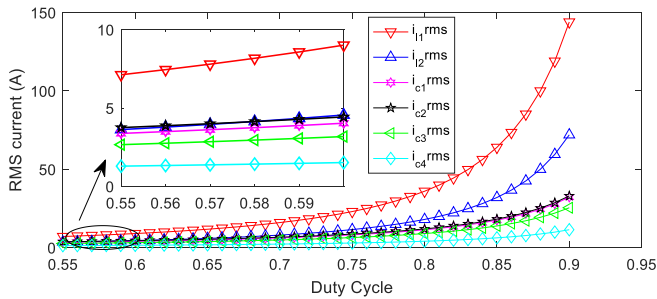$$I_{c4} = \sqrt{\left(-\frac{v_{c2} + v_{c4}}{R}\right)^2 + \left(\frac{i_{l1} - i_{l2}}{2}\right)_{RMS}^2 (D_2')} \tag{46}$$

where $S = (-\frac{v_{c2} + v_{c4}}{R} - (\frac{i_{l1}}{2})_{RMS})^2$.

The diagrams for the RMS current of the capacitors and inductors for different duty cycles are shown in Fig. 7.

C. THE VOLTAGE AND CURRENT STRESS OF THE SWITCHES

The peak values of the voltage and current stress of the switches are given as:

$$I_{SW1} = I_{SW2} = \frac{G^2 V_{in}}{R} \tag{47}$$

FIGURE 7. The RMS current of capacitors and inductances in converter with proposed switching method.

TABLE 1 Calculated Efficiency of the Converter Employing the Proposed and Conventional Switching Methods for Different Voltage Gain and Output Power

v_{out}/v_{in}	Output power (W)	Efficiency(%)	
		proposed	*conventional*
140/18	100	94.01	91.82
	130	93.37	91.22
	160	92.86	90.7
	200	91.93	90.01
180/18	100	93.7	91.11
	130	93.24	90.62
	160	92.54	89.86
	200	91.86	89.23
240/18	100	93.09	89.63
	130	92.71	89.24
	160	91.99	88.56
	200	91.3	87.94

TABLE 2 Hardware Specifications

Parameter	Value	Components	Value
Input voltage (V_{in})	18 V	C_1, C_2, C_3, C_4	100 μF
Output voltage (V_{out})	180 V	L_1	580 μH
Output power	160 W	R_{L1}	0.2 Ω
Switching frequency (f_s)	30 kHz	L_2	420 μH
Switch-on resistance (R_{on})	0.04 Ω	R_{L2}	0.08 Ω
Diode forward voltage (V_f)	1.5 V		

$$V_{SW1} = \frac{V_{in}}{D'_1} \tag{48}$$

$$V_{SW2} = V_{in}\left(\frac{G}{2} - \frac{1}{D'_1}\right) \tag{49}$$

(47)-(49) show that for a given G, D_1 has no effect on the current stress but V_{sw} depends on D_1. Lower voltage stress is desirable which is achieved while $D_1 = 1 - 4/G$. In this condition, D_1 is equal to D_2 ($D_1 = D_2$) and both switches have the same voltage stress. This condition is shown in Fig. 6.

D. THE CONVERTER POWER LOSS AND EFFICIENCY

The next criteria are the converter power loss and efficiency. The only part of losses that is affected by D_1 is the conduction and switching losses (P_{COND} and P_{SW}) of the switches. According to [19], P_{COND} is given by (50) and P_{sw} is calculated by (51);

$$P_{COND(S)} = P_{COND(S1)} + P_{COND(S2)} = R_{on}I_{L1}^2 \tag{50}$$

$$P_{SW} = P_{SW1} + P_{SW2} = \frac{G^2\left[G^2D'^2_1 - 4GD_1D'_1 + 8\right]}{D'^2_1}\left[\frac{V_{in}}{R}\right]^2 f \tag{51}$$

where R_{on} is the conducting resistance of the switches and is assumed to be the same for both. (50) shows that P_{COND} is not related to D_1. But (51) indicates that for minimizing and balancing the power loss of switches D_1 should be equal to D_2 ($D_1 = D_2$).

The above discussion concludes that balancing voltage stress of the switches is achieved when $D_1 = D_2$. In this condition, other merits are obtained such as:

- The balanced power loss of the switches.
- Lower input current ripple (not the lowest ripple is achieved)
- Ease of implementation. Conventional pulse width modulation (PWM) control ICs can be used to generate the commands.

For common and suggested switching methods, the converter efficiency in the non-ideal mode is obtained. Diode voltage drop v_f, inductance resistance r_l, and resistance of switches r_{on}, were selected as non-ideal elements. The steady-state output voltage using the proposed switching method is given by:

$$v_{out} = \frac{2v_{in}\left(\frac{D'_1 + D'_2}{D'_1 D'_2}\right) - 4v_f}{1 + (a)(2r_{on}(b) + 2r_l(c)) + (e)(2r_{on}(m))} \tag{52}$$

where $a = \frac{D'_1 D'_2 + D'^2_2 - D'_1 - D'_2}{D'_1 D'^2_2}$, $b = \frac{D'_1 + D'^2_2 + D'_1 D'_2}{RD'_1 D'_2}$, $c = \frac{D'_1 + D'_2}{RD'_1 D'_2}$,

$e = \frac{D'_2 - 1}{D'_1 D'_2}$, $m = \frac{D'_1 - D'^2_1 - 4D'_1 D'_2 - 3D'^2_2 + 3D'_2}{RD'_1 D'_2}$.

Employing the conventional switching strategy, the output voltage is given by:

$$v_{out} = \frac{2\frac{v_{in}}{DD'} - 4v_f}{1 - \left(\frac{1-2D}{DD'^2}\right)\left(\frac{2(r_{on}+r_l)}{RDD'}\right) - \left(\frac{1-2D}{DD'}\right)\left(\frac{2r_l}{RD}\right)} \tag{53}$$

The calculated values for the proposed and conventional switching methods are given in Table 1, which demonstrates the advantages of the proposed switching strategy.

III. STATE-SPACE AVERAGING MODEL AND SMALL-SIGNAL ANALYSIS

In this section, the converter dynamic model using the presented switching method is described. The following assumptions are valid throughout the entire analysis:

1) The passive components, L and C are lossless linear, time-invariant, and frequency independent.
2) The capacitor values are the same.
3) Semiconductor switches are ideal.
4) The input voltage V_{in} is an independent voltage source.

5) The natural time constant of the converter is much larger than one switching period.

6) To provide a closed and general form of the proposed approach, the diode voltage drop is neglected. Eliminating the voltage drop does not affect the controller performance.

According to the discussion in the previous section, duty cycles of both switches are considered the same ($d_{(t)} = d_{1(t)} = d_{2(t)}$).

Using the relations governed the converter ((1)-(30)), state-space models in the three states can be described; state I: $K\dot{X} = A_1 X + B_1 U$, state II: $K\dot{X} = A_2 X + B_2 U$, state III: $K\dot{X} = A_3 X + B_3 U$.

Large signal-averaged equations $K\dot{X} = AX + BU$ can be determined by the circuit averaging technique wherein $A = (1-d)A_1 + (1-d)A_2 + (2d-1)A_3$ and $B = (1-d)B_1 + (1-d)B_2 + (2d-1)B_3$.

$$X = \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \\ v_{C3} \\ v_{C4} \end{bmatrix}, \quad K = \begin{bmatrix} L_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 & 0 & 0 \\ 0 & 0 & C_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & C_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & C_3 & 0 \\ 0 & 0 & 0 & 0 & 0 & C_4 \end{bmatrix}, \quad B = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{54}$$

$$A = \begin{bmatrix} \frac{-R_d d'}{2} & \frac{R_d d'}{2} & 1-d & -d' & \frac{d'}{2} & \frac{d'}{2} \\ \frac{R_d d'}{2} & -R_d d' & 2d-2 & \frac{3}{2}d' & -d' & \frac{d'}{2} \\ -d' & 2d' & 0 & 0 & 0 & 0 \\ d' & -\frac{3}{2}d' & 0 & \frac{-1}{R} - \frac{d'}{2R_d} & \frac{d'}{2R_d} & \frac{-1}{R} \\ \frac{-d'}{2} & d' & 0 & \frac{d'}{2R_d} & \frac{-d'}{R_d} & \frac{d'}{2R_d} \\ \frac{d'}{2} & \frac{-d'}{2} & 0 & \frac{-1}{R} & \frac{d'}{2R_d} & \frac{-1}{R} - \frac{d'}{2R_d} \end{bmatrix} \tag{55}$$

where $d' = (1-d)$.

Assuming small perturbation for the inputs and state variables, the small-signal model and the open-loop transfer function in the s-domain of the small-signal model around a specific equilibrium point, defined by the steady-state value of the duty-cycle D can be obtained. The control-to-output transfer function ($G_{vd} = \hat{v}_{out}/\hat{d}$) and input-to-output transfer function ($G_{vg} = \hat{v}_{out}/\hat{v}_{in}$) are calculated by (56) and (57).

$$G_{vd} = \frac{n_{d4}S^4 + n_{d3}S^3 + n_{d2}S^2 + n_{d1}S^1 + n_{d0}}{d_4 S^4 + d_3 S^3 + d_2 S^2 + d_1 S^1 + d_0} \tag{56}$$

where, $n_{d4} = 0$, $n_{d3} = -2CI_L L_1 L_2$, $n_{d2} = -RCL_2 V_{out}(D-1)$, $n_{d1} = -2RI_L(4L_1 + L_2)(D-1)^2$, $n_{d0} = RV_{out}(-2D^3 + 6D^2 - 6D + 2)$, $d_{d4} = 6R\,C^2\,L_1 L_2$, $d_{d3} = 8CL_1 L_2$, $d_{d2} = 2RC(D-1)^2(13L_1 + 4L_2)$, $d_{d1} = 8(D-1)^2\,(4L_1 + L_2)$, $d_{d0} = R(2D^4 - 8D^3 + 12D^2 - 8D + 2)$.

$$G_{vg} = \frac{n_{g4}S^4 + n_{g3}S^3 + n_{g2}S^2 + n_{g1}S^1 + n_{g0}}{d_4 S^4 + d_3 S^3 + d_2 S^2 + d_1 S^1 + d_0} \tag{57}$$

where, $n_{g4} = 0$, $n_{g3} = 0$, $n_{g2} = 2RCL_2(D-1)$, $n_{g1} = 0$, $n_{g0} = 4R(1-D)^3$.

Pole-zero maps are plotted for G_{vd} in Fig. 7. They are used for selecting passive elements, analysing the impact of load resistance on dynamic behaviour as well as duty ratio. The converter characteristics used in this section are the same as the prototype specifications described in the result section.

A. SELECTING PASSIVE COMPONENTS

Generally, the main criteria to choose the proper values of L and C are as follows [23]:

- Satisfactory ripple performance;
- Influence on control performance;
- Proper quality factor and damping factor;
- Sufficient phase margins for close loop control;
- Resonant frequency far away from the switching frequency for stability;
- The right half plane (RHP) poles far away from the origin;
- Smaller passive components (lower costs and sizes)

It should be considered that the determining L and C values are related to the design stage of the converter according to the recommended working conditions and operating point. As shown in Fig. 7, the pole-zero map of G_{vd} includes two RHP zeros. The presence of RHP zeros, generally, tends to destabilize the wide-bandwidth feedback loops, implying high-gain instability, may cause slower transient response and impose control limitations. As a result, the feedback design to achieve an adequate phase margin gets more difficult and the system is sensitive to the controller's delay [24]. The closer RHP zeros to the origin, the more control limitations, and always there is a trade-off between closed-loop output responses and the zero direction of the open-loop system.

The effect of C on the pole and zero locations is shown in Fig. 8(a). It shows the shifting of poles and dominant RHP zero toward the imaginary axis as C increases from 100 μF to 1000 μF. The shifting of zero toward the imaginary axis increases the non-minimum-phase undershoot, and the shifting of poles increases the system settling time and oscillatory response. Therefore, it is important to carefully select the values of passive elements to achieve a good compromise between oscillatory response and non-minimum-phase effect. Fig. 8(b) depicts that dominant RHP zero and pair poles do not change significantly as L_1 varies from 100 μH to 700 μH. Therefore, larger L_1 is desirable to mitigate input current ripple.

L_2 shows the same effect as C (Fig. 8(c)). So, according to the above description, a smaller L_2 can help to improve the control performance of the system.

### B. IMPACT OF STEADY-STATE OPERATING DUTY RATIO

Fig. 7(d) shows the pole-zero map of G_{vd} in various operating points regarding changes in D (0.54, 0.64, and 0.74). Observation of the pole-zero map shows that the dominant pair of the complex poles move closer slightly to the real axis as D increases, resulting in heavier damping effects. On the other hand, RHP zeroes shift also closer to the origin, therefore the achievable control performance is degraded.
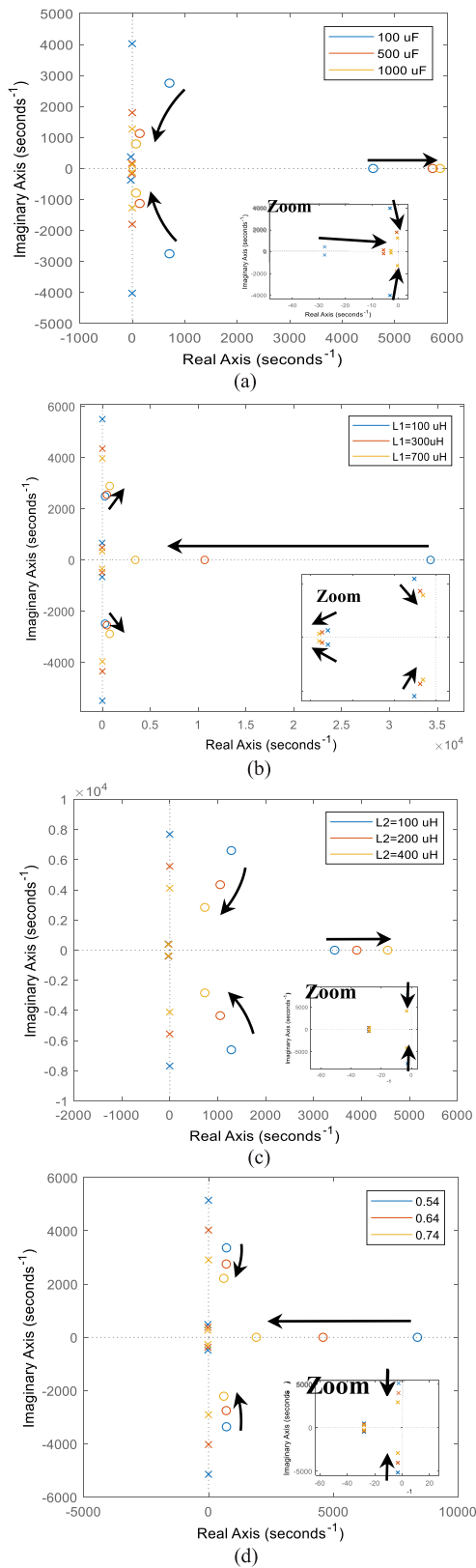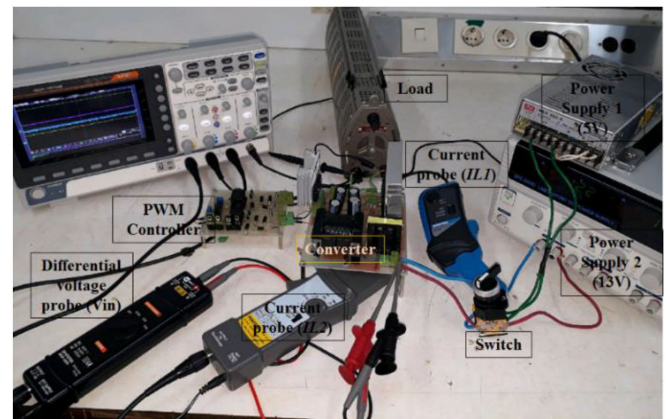
FIGURE 8. Pole-zero map of G_{vd} for different values of (a) capacitance, (b) L_1, (c) L_2, and (d) duty ratio.
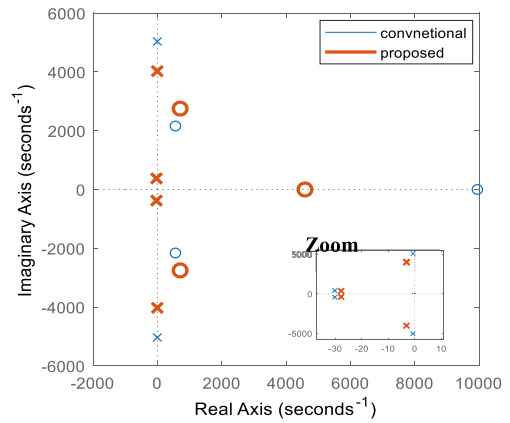
FIGURE 9. Comparison of the G_{vd} pole-zero map for the proposed and conventional switching strategies.
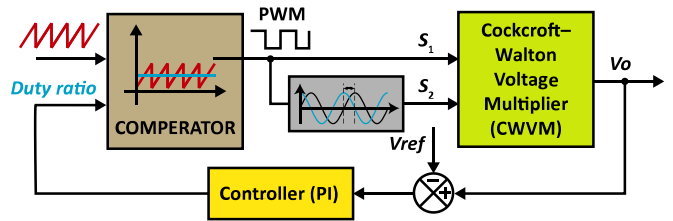
FIGURE 10. Block diagram of the proposed control system.

FIGURE 11. The developed laboratory experimental setup.

C. COMPARISON TO THE CONVENTIONAL SWITCHING METHOD IN TERMS OF DYNAMIC PERFORMANCE

Using the specifications of the prototype Table 2 the G_{vd} pole-zero plot for two conditions (using proposed and conventional switching strategies) are shown in Fig. 9. It shows that, although the system has RHP zeroes for both methods but the dominant RHP zeroes while using the proposed method are farther from the origin which imposes better control aspects. The locations of dominant poles are approximately the same for both methods, however dominant pair poles for the proposed switching method are marginally farther than the dominant pair poles for the conventional switching method.

D. CONTROLLER DESIGN

The purpose of designing the controller, proportional-integral (PI) controller in this paper, is to track voltage reference (v_{ref}) with zero-state error and good transient response. Besides, an appropriate stability margin for the system against parameter changes must be obtained.

A larger amount of error changes the duty cycle through the K_P and K_I coefficients of PI controller and then the output voltage is regulated. The block diagram of the control system is shown in Fig. 10.

IV. EXPERIMENTAL VERIFICATIONS

An experimental prototype of the converter (Fig. 11) was built with the specifications described in Table 2. Several experiments are carried out which the results are shown here to validate the proposed method and dynamic analysis.

A. EXPERIMENTAL RESULTS FOR THE STEADY-STATE OPERATION

The experimental results for the steady-state operation of the converter using the proposed and the conventional switching strategy are shown in Fig. 12. To provide $V_{out} = 180$ V, D is adjusted to 0.64 for the proposed strategy and 0.76 for the conventional method. The converter output and input voltages, as well as inductors currents, are shown in Fig. 12. Respectively, the current waveforms are as expected (Fig. 5). The applied gate-source voltages (V_{gs}), as well as voltage across the switches (V_{ds}), are shown. It shows that in the proposed strategy voltage across the switches are the same and equals 45 V while $V_{sw1} = 22$ V and $V_{sw2} = 72$ V for the conventional method. Balanced voltage stress is one of the main advantages of the proposed strategy.

B. DYNAMIC MODEL VALIDATION

To validate the dynamic model, computer simulations are conducted and compared with the detailed model in ideal conditions. In Fig. 13, simulation results are subject to a step change of duty ratio from 0.55 to 0.64 by the detailed switching circuit model (Fig. 13(a)) and the small-signal model (Fig. 13(b)) are shown. The extracted model shows good consistency with the detailed model in the steady-state and transient conditions. For the next experiment, the parasitic elements are included in the model. The main parasitic components of the converter including inductor resistance (R_{L1} and R_{L2}), switch conducting resistance (Ron) and diode forward voltage (V_f) are considered and the non-ideal transfer functions are extracted. Fig. 14(a) shows the experimentally obtained response of V_{out} to a step change in V_{in} from 18 V to 13 V. The simulation result for the model is shown in Fig. 14(b). The experimental and model simulation results for a step change in duty ratio from 0.55 to 0.64 are shown in Fig. 15(a) and Fig. 15(b) respectively. The model results were found to be in good agreement with the experimental step responses.
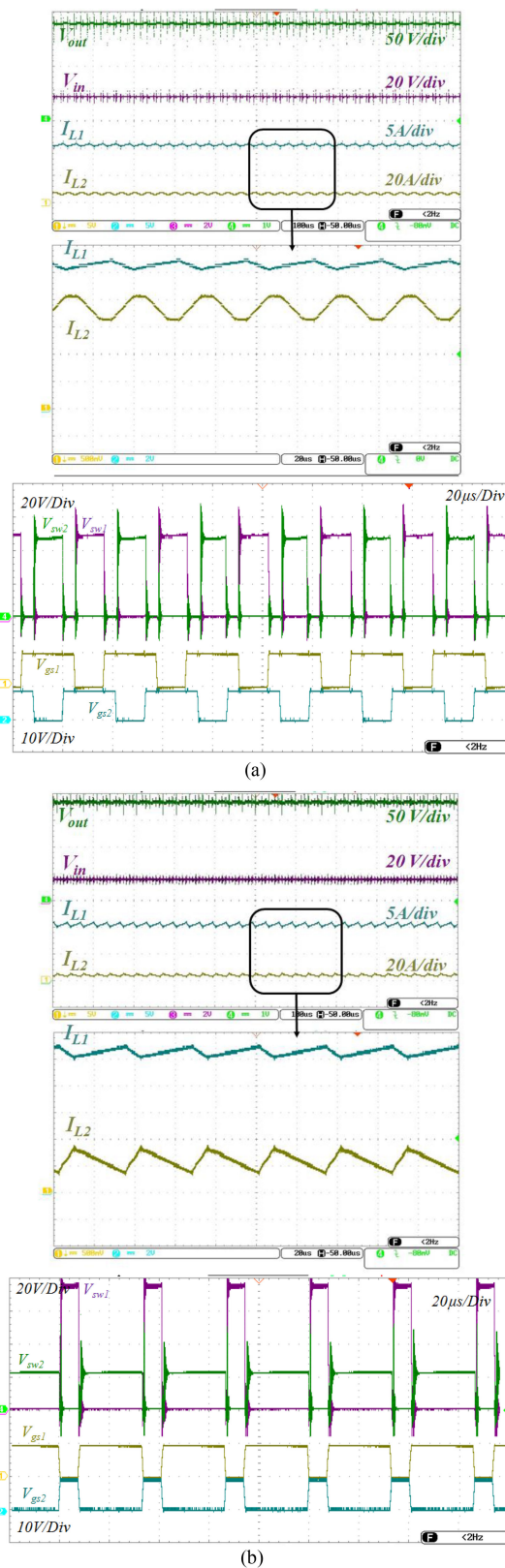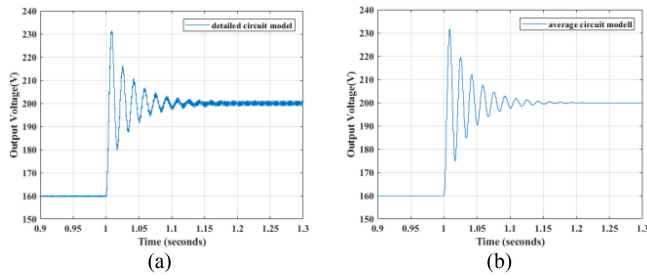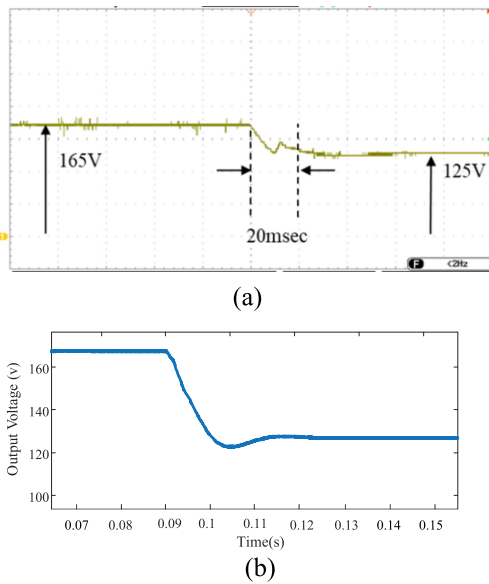

FIGURE 12. Experimental results for the steady-state operation of the power converter using (a) the proposed switching strategy and (b) the conventional switching strategy.

FIGURE 13. Simulation results for the transient response of the output voltage subject to a step change of D from 0.55 to 0.64. (a) Detailed model and (b) small-signal model.


FIGURE 14. Transient response for the output voltage due to a step-change in V_{in} from 18 V to 13 V. (a) Experimental (50 Volt/div., 20 msec./div) and (b) model simulation.
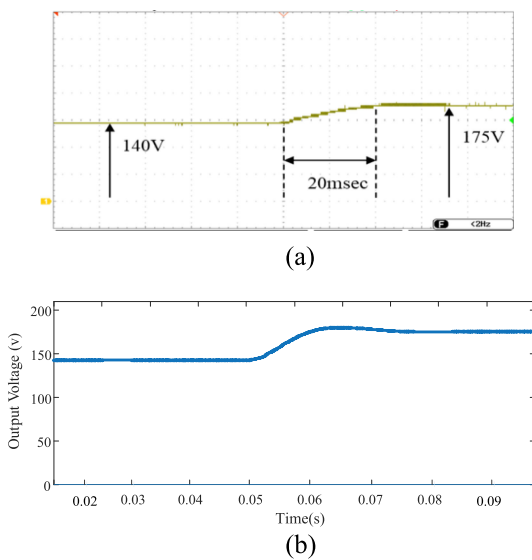
FIGURE 15. Transient response for output voltage due to a step change in $d_{(t)}$ from 0.55 to 0.64. (a) Experimental (50 Volt/div., 10 msec./div) and (b) model simulation.

TABLE 3 The Scenarios to Evaluate the Controllers of Converter

Scenarios	time	description
Scenario1	$0 < t \leq 0.3$	$V_{in} = 24V, V_{ref} = 250V, R_{load} = 200\Omega$
Scenario2	$0.3 < t \leq 0.6$	$V_{in} = 24V, V_{ref} = 200V, R_{load} = 200\Omega$
Scenario3	$0.6 < t \leq 0.9$	$V_{in} = 20V, V_{ref} = 200V, R_{load} = 200\Omega$
Scenario4	$0.9 < t \leq 1.2$	$V_{in} = 20V, V_{ref} = 200V, R_{load} = 150\Omega$
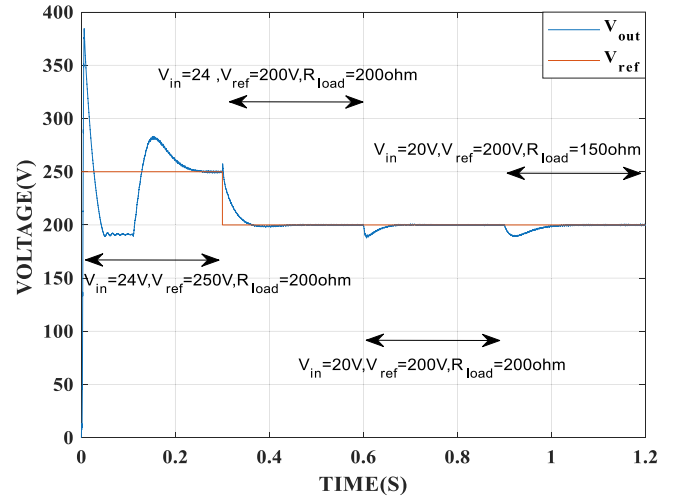
FIGURE 16. Performance of the proposed control scheme.

C. DYNAMIC RESPONSE

To validate the performance of the designed PI controller, the converter was evaluated in the simulation environment based on the listed scenarios in Table 3. The output voltage changes are shown in Fig. 16. The controller tracks the desired reference voltage with a fast transient response in presence of load changes.

V. CONCLUSION

This study proposed a switching strategy based on adjusting the overlap interval of commands for two switches of a high step-up dc-dc power converter topology with CWVM. Compared to the conventional strategy, the main advantages of this method are 1) Balancing the voltage stress and power loss of the power switches. This improves the thermal management of the converter; 2) Reducing the ripple of the input current; 3) comparing the pole-zero maps showed that, although the converter is a non-minimum-phase system, the RHP zeros are farther from the origin (compared to the conventional strategy). This mitigates the negative effect of the non-minimum phase on the dynamic behaviour and simplifies the procedure of the controller design. The mathematical relations for the small-signal model and control-to-output voltage-transfer functions are derived. The control-to-output transfer function showed the presence of an RHP zero, which causes the output to decrease initially before rising towards its new steady-state value when a step increase in control input is applied. The identified RHP zero cannot be eliminated by adjusting the

parameters, but its effect can be reduced by reducing the capacitance. As illustrated by the design-oriented analysis, the analytical results can help designers to select proper power converter components and to understand system limits. Reducing the RHP effect by adjusting system parameters; however, is always accompanied by some negative effects such as increases in losses, ripples, and system settling time. A prototype of the power converter was built and tested to validate the proposed switching strategy and small-signal models. Experimental results show well agreement concerning the theoretical predictions.

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