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Model Predictive Controllers With Capacitor Voltage Balancing for a Single-Phase Five-Level SiC/Si Based ANPC Inverter

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ABSTRACT Employing both high bandwidth (HBW) controller and wide bandgap (WBG) devices in the structure of converters improve the system size, performance, and efficiency. In this paper, HBW model predictive controllers (MPCs) are proposed, with both fixed and unfixed switching frequencies, to control a single-phase five-level hybrid active neutral-point-clamped (ANPC) inverter. A hybrid modulation technique is considered in this paper, in which some of the switches are modulating with high frequency. Therefore, Silicon-Carbide (SiC) MOSFETs are employed in the converter structure to increase the switching frequency and consequently reduce the filter size and increase converter power density. To have the functionality of multilevel output voltage, some restrictions are defined in the adopted MPC with unfixed switching frequency. In the MPC with the constant switching frequency, predefined switching sequences are employed for all sectors. Moreover, to control the neutral point (NP) voltage, the applied times of both small voltage vectors are sets through a cost function. Finally, the simulation and experimental results prove the ability of both proposed methods to control the voltages of the load and NP.

INDEX TERMS Model predictive control, cost function, DC-AC converters, multilevel converter, voltage control.

NOMENCLATURE

V_{DC}	DC supply voltage
v_{ab}	Output voltage of the converter
v_d	Load voltage
v_p	Voltage of upper dc-link capacitor
v_n	Voltage of lower dc-link capacitor
v_{np}	Voltage of Neutral point
v_{ref}	Reference voltage
v_x	Output vector x
v_y	Output vector y
i_o	Neutral point current
i_p	Current of the upper dc-link capacitor
i_n	Current of the lower dc-link capacitor
i_c	Current of the filter inductor
i_d	Current of the filter capacitor
i_f	Load current
i_{Rn}	Current of the resistor in parallel with lower dc-link capacitor
L_c	Filter inductance
R_c	Resistance of filter inductor
R	Load resistance
R_n	Resistor in parallel with lower dc-link capacitor
C_d	Filter capacitor
C_p	Upper dc-link capacitor
C_n	Lower dc-link capacitor
f_{sw}	Switching frequency
f	Reference frequency
T_s	Step time
t_x	Applied time of vector x
t_y	Applied time of vector y
t_{y1}	Applied time of first small vector

t_{y2}	Applied time of second small vector
λ	Weighting factor
S_k (k = 1 …8)	Switch number
V_i (i = 1 …8)	Output voltage vector

I. INTRODUCTION

With increasing the penetration of renewable energy and energy storage systems, the demand for power converters as a key role is rising [1]–[3]. Among these applications, single-phase converters are employed in photovoltaic (PV), electric railway traction, and power factor correction applications [4]–[9]. Compared to the conventional two-level converter, multilevel converters have become more interested due to their superior characteristics, such as lower *dv/dt*, improved current and voltage total harmonic distortion (THD), lower common-mode voltage, and smaller filter inductance [10], [11]. The three main structures of multilevel converters are Neutral-point-clamped (NPC), flying capacitors (FC), and cascaded H-bridge (CHB) converters. One interesting topology for single-phase application is the 5-level single-phase NPC converter, which presents high efficiency and compact design compared to a 3-level converter [6], [12], [13]. One of the derived topologies from NPC structure is a 5-level single-phase hybrid active NPC converter [6], in which just eight switches are utilized. Moreover, this structure presents the ability of hybrid switching frequency to improve the efficiency of the converter. Meanwhile, employing recent emerging of wide bandgap (WBG) switches such as SiC MOSFETs can improve the efficiency and reduce the converter size.

Apart from the topology of the converter, controlling the converter is a determining issue. A wide variety of control strategies have been discussed for single-phase converters, such as proportional integral derivative (PID), and proportional resonant (PR) and current hysteresis controls, etc [14]–[17]. However, these linearized controllers suffer from slow dynamic responses. Therefore, the implementation of novel and complex control algorithms such as model predictive control (MPC) have been considered and proposed in the literature with the release of advanced and fast microprocessors, digital signal processors (DSPs), and field-programmable gate array (FPGA) platforms in the market [12], [17]–[24]. The MPC strategy, as an interesting alternative controller, utilizes the mathematical model of the system to predict the behavior of converters. In fact, the controller can predict the future behavior of converters based on the discrete characteristics of the power electronic converter and the system output values. A cost function is also employed to determine the next switching state of the converter to find the optimum operation mode. Meanwhile, this process is repeated at the next sampling cycle [12], [17], [25]. One of the popular MPC strategies is finite control set MPC (FCS-MPC), in which the output voltage vectors of a converter are considered as the control inputs to handle the optimal control problem [12], [26]–[28]. The most advantageous features of FCS-MPC are its fast-dynamic response, the simplicity of its implementation, and the ability to integrate advanced control objectives in the design of its cost function [12], [17]. Moreover, the need for switching modulators and inner control loops and their delays are eliminated by employing the FCS-MPC. Therefore, the system can be operated with higher bandwidth and faster performance [29]. However, this FCS-MPC strategy employs only one output vector of the converter in every control period. Thus, the switching frequency of the converter is unfixed [12], [13], which can be counted as the main disadvantage of FCS-MPC.

To deal with the unfixed switching frequency of MPCs, several techniques, e.g., optimal switching sequence, have been presented for single-phase converters [12], [13], [17], [30]. In [13], an MPC based on the optimal switching sequence has been proposed for a single-phase H-bridge NPC. However, NP voltage balancing is not considered. The same MPC with controlling the NP voltage has been modified in [12]. Ref [17] developed an MPC with a fixed switching frequency for a T-type inverter, in which the idea of space vector pulse-width modulation (SVPWM) is utilized by defining switching patterns in different sectors. In [30], an MPC with a fixed switching frequency based on the SVPWM has been proposed. However, the SVPWM block is included in the controller loop, which leads to system delay and sluggish dynamic performance. Although MPC methods have been upgraded to track different setpoints, modifications still are required based on converter topologies and desired factors.

This paper investigates the utilization of HBW control system for a single-phase 5-level hybrid SiC/Si ANPC topology with high switching frequency. The control system includes two different FCS-MPCs with unfixed and constant switching frequencies. In the first method to improve the THD of output voltage, some restrictions regarding the selection of the output voltage vectors are defined. With these restrictions, the waveform of the output voltage is changed between defined levels. Considering the switching frequency is not fixed in the first method, designing the filter would be challenging and leads to a large output current ripple. Therefore, an enhanced MPC with constant switching frequency is utilized, which is based on the idea of SVPWM [17] for each sector, a predefined switching sequence is defined. To regulate the NP voltage, the effect of different output vectors is studied, and a sub cost function is allocated in both methods. A prototype of the converter is used to experimentally validate the proposed control schemes, wherein 50 kHz switching frequency is implemented by an FPGA. In summary, the main contributions of this paper are as follows:

1) Proposing two high bandwidth MPCs for a 5-level high-frequency SiC/Si inverter.
2) Developing unfixed switching frequency MPC (adopted MPC) considering the converter restrictions and switching states to achieve an improved output voltage waveform.
3) Proposing a modified MPC with constant switching frequency based on the SVPWM idea for the considered structure to obtain staircase output voltage.
4) Embedding the NP voltage balancing algorithm in both proposed MPCs.

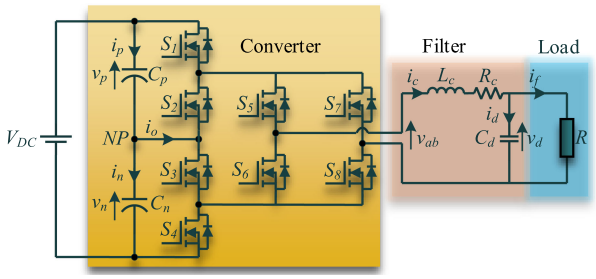

FIGURE 1. The schematic of 5-level single-phase ANPC inverter with a constant dc source, a filter and a load.

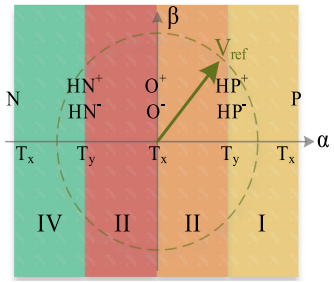

FIGURE 2. The voltage vector diagram of the single-phase 5-level converter.

TABLE 1. The Switching States of 5-Level Single Phase ANPC

Vector	State	v_{ab}	Switching states							
			S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
V_1	P	V_{DC}	1	0	0	1	1	0	0	1
V_2	HP^+	$V_{DC}/2$	1	0	1	0	1	0	0	1
V_3	HP^-	$V_{DC}/2$	0	1	0	1	1	0	0	1
V_4	O^+	0	0	1	1	0	1	0	0	1
V_5	O^-	0	0	1	1	0	0	1	1	0
V_6	HN^+	$-V_{DC}/2$	1	0	1	0	0	1	1	0
V_7	HN^-	$-V_{DC}/2$	0	1	0	1	0	1	1	0
V_8	N	$-V_{DC}$	1	0	0	1	0	1	1	0

5) Digital model-based implementation of the proposed MPCs through FPGA.

The rest of the paper is organized as follows. The 5-level single-phase ANPC inverter structure and mathematical modeling are presented in section II. Section III presents the proposed model predictive control algorithms. The simulation and experimental results for both methods are demonstrated in section IV. Finally, section V concludes the study.

II. SYSTEM STRUCTURE AND MODELING

The general schematic of the system based on the single-phase hybrid active NPC is shown in Fig. 1. The system consists of a constant dc source (V_{DC}) as a supplier, the converter, an LC filter, and a load.

In the structure of the converter, eight power switches (S_k, k = 1, 2 …, 8) and two dc-link capacitors (C_p and C_n) are utilized. Five voltage levels at the output of the converter can be constructed by employing different combinations of switching states. To reach a hybrid switching frequency, eight switching states can be utilized, which are listed in Table 1. During the whole positive half cycle, S_5 and S_8 are conducting, and the conditions of S_1-S_4 are altered to reach different output voltage levels. Meanwhile, S_6 and S_7 are in the on-state condition in the negative half cycle, and S_1-S_4 are modulating with higher switching frequency. Therefore, the switching frequency of S_5-S_8 is fundamental or 50 Hz in this study. Moreover, two different switch technologies, including SiC and Si MOSFETs, are employed due to devices switching frequencies.

Based on the magnitude of the reference waveform, the voltage vector diagram of a 5-level converter can be divided into four sectors. Fig. 2 shows these four sectors with respective voltage vectors of each one. The voltage vector diagram is comprised of two large vectors P and N, two zero vectors O^+ and O^-, four small vectors HP^+, HP^-, HN^+, and HN^-. The large and zero vectors do not have any influence on the NP voltage. Meantime, the small vectors can change the NP voltage. When the small vectors are employed, the current closes its path through one of the dc-link capacitors.

To develop MPC, the mathematical modeling of the converter, including the filter and the load in AC and DC sides, is vital. Based on the circuit of Fig. 1, the relation between the output voltage of the converter (v_{ab}), the current of the filter inductor (i_c), and the voltage across the load (v_d) can be written as follows:

$$v_{ab} = L_c di_c/dt + R_c i_c + v_d \tag{1}$$

where L_c and R_c are the inductance and resistance of filter inductor, respectively. The relation between the currents of filter inductor, filter capacitor (i_c), and load (i_f) can be noted as follows:

$$i_c - i_f = i_d = C_d dv_d/dt \tag{2}$$

where C_d is the value of the filter capacitor. Therefore, the converter output voltage and current can be shown in the state-space form as follows:

$$\frac{d}{dt}\begin{bmatrix} i_c \\ v_d \end{bmatrix} = A\begin{bmatrix} i_c \\ v_d \end{bmatrix} + B\begin{bmatrix} v_{ab} \\ i_f \end{bmatrix}$$
$$A = \begin{bmatrix} -\frac{Rc}{Lc} & -\frac{1}{Lf} \\ \frac{1}{Cd} & 0 \end{bmatrix} B = \begin{bmatrix} \frac{1}{Lf} & 0 \\ 0 & -\frac{1}{Cd} \end{bmatrix} \tag{3}$$

For the DC part of the converter, the NP current (i_o) is equal to the current of the filter inductor (i_c), whenever small vectors are employed. The effects of small vectors on the NP voltage variations are shown in Table 2. Moreover, the voltage of upper and lower dc-link capacitors (v_p, v_n) based on the current of dc-link capacitors (i_p, i_n) can be found through the following equations:

$$i_p = C_p dv_p/dt \tag{4}$$

$$i_n = C_n dv_n/dt \tag{5}$$

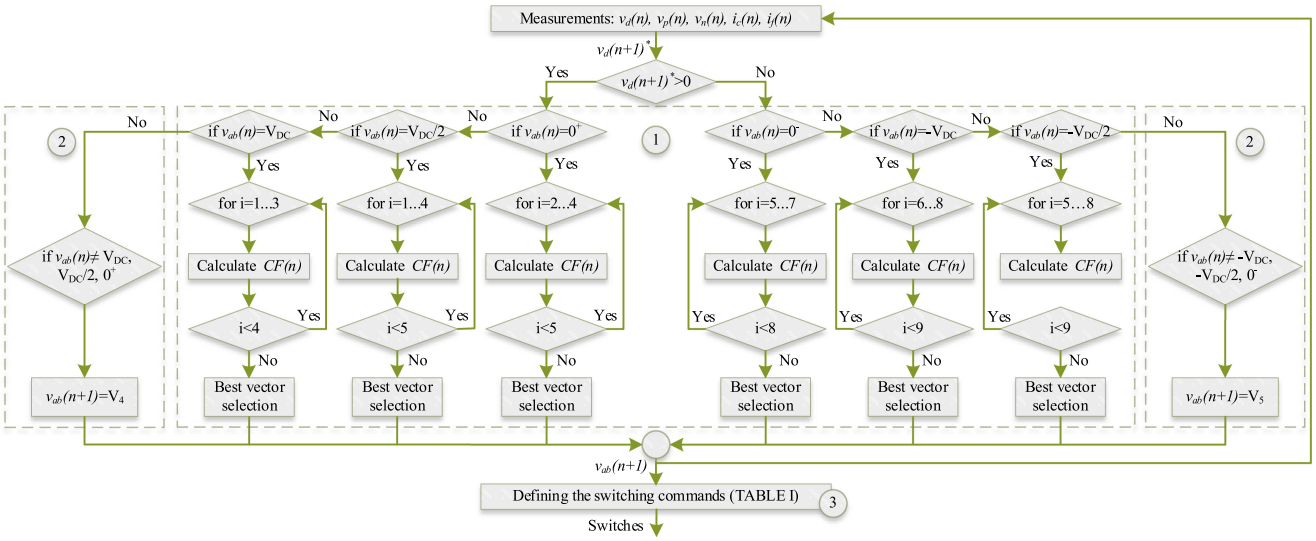

FIGURE. 3. The flowchart of the adopted MPC.

TABLE 2. The Effect of Small Vectors on the NP Voltage

Vector	Output current	$v_{NP}=v_p-v_n$
V_2	$i_c>0$	↓
	$i_c<0$	↑
V_3	$i_c>0$	↑
	$i_c<0$	↓
V_6	$i_c>0$	↑
	$i_c<0$	↓
V_7	$i_c>0$	↓
	$i_c<0$	↑

where C_p and C_n are the capacitance value of dc-link capacitors. In addition, the NP voltage is indicated as:

$$v_{NP} = v_p - v_n \tag{6}$$

III. MPC SCHEMES

The main objects of the control method are to appropriately set the output voltage of the converter (v_{ab}) so that the voltage across the load (v_d) can follow the reference voltage and to control the NP voltage variation. In this section, two different MPC controls are presented.

A. ADOPTED MPC

The cost function of adopted MPC for 5-level ANPC converter is defined as follows:

$$\begin{aligned} CF(n) = &\left|v_d(n+1)^* - v_d(n+1)\right| \\ &+ \lambda_1(\left|i_c(n+1) - i_f(n)\right|) \\ &+ \lambda_2(\left|v_p(n+1) - v_n(n+1)\right|) \end{aligned} \tag{7}$$

where λ_1 and λ_2 are weighting factors to reduce the current ripple and to balance the NP voltage, respectively. The defined cost function is comprised of three subfunctions. The main subfunction is the first part, which tries to find the best vector for tracking the reference voltage. The purpose of the second part of the cost function is to reduce the current ripple at the filter inductor by comparing the output current of the converter with the filtered load current. The third subfunction of the cost function is employed to regulate the NP voltage. Each vector has a different effect on the value of cost function through (3), where v_{ab} is replaced with the output voltage vectors. As mentioned earlier, the small vectors have different effects on the NP voltage. The dc-link capacitor voltages for the small vector can be obtained as follows:

$$\begin{aligned} v_p(n+1) &= v_p(n) + i_p(n) \times T_s/c_p \\ v_n(n+1) &= v_n(n) + i_n(n) \times T_s/c_n \end{aligned} \tag{8}$$

where T_s is the discrete step time.

The flowchart of the proposed MPC is shown in Fig. 3. The flowchart is divided into two sections based on the value of the reference voltage. The reasons are 1) to keep the switching frequency of S_5, S_6, S_7, and S_8 at 50 Hz and to prevent any unwanted transitions during zero-crossing between positive and negative half cycle, 2) to decrease the computational time of the controller implementation. Besides, some restrictions are defined to have the functionality of multilevel output voltage. These restrictions can be found through the four subbranches in each section, in which, based on the previous output voltage vector, the subbranch is chosen (block 1). For example, when $v_{ab}(n) = V_{DC}$, the next applied vector can be the same vector or the vectors with half of the dc-link voltage ($v_{ab}(n+1) = V_{DC}$ *or* $V_{DC}/2$). Otherwise, the output voltage of the converter changes from V_{DC} to 0, which increases the current ripple at the filter inductor, the magnitude of harmonic contents, and THD of the output voltage. In each subbranch, the cost function (7) is calculated for considered output voltage vectors, where i defines V_i as the output voltage vector that are listed

TABLE 3. The Vector Sequences of MPC With Constant Switching Frequency

Sector	Vector sequence
I	P-HP^{+*}-P-HP^{-**}-P
II	O^{+}-HP^{+*}-O^{+}-HP^{-**}-O^{+}
III	O^{-}-HN^{-*}-O^{-}-HN^{+**}-O^{-}
IV	N-HN^{-*}-N-HN^{+**}-N

*time duration $= t_{y1}$
**time duration $= t_{y2}$

in Table 1. In the next step, the output voltage vector with minimum related cost function is selected to apply (block 1). This state is shown as the best vector selection in the flowchart. Finally, the commands of switches are determined by defining the switching commands function (block 3). Besides, the employed output voltage vector is used to define the next output vector. Moreover, two subsections are employed for the transition during zero-crossing to apply a zero-voltage output vector (V_4 or V_5) in each section (block 2).

B. ENHANCED MPC WITH CONSTANT SWITCHING FREQUENCY

In the previous MPC, the switching frequency is unfixed, which leads to large output current ripple, and consequently, the current harmonics are distributed in a wide range of frequency. Meanwhile, employing the idea of SVPWM to reach a constant switching frequency can reduce the output current ripple and having current harmonics at switching frequency and multiple of it [17]. Moreover, increasing the switching frequency of the converter reduces the size of the passive components of the filter. Decreasing the size of the inductor and capacitor of the filter reduces the reactive power consumption of the filter and consequently reduces the phase difference between the input and output voltages of the filter. Therefore, it can be assumed the v_{ab} and v_d are in phase.

Considering the voltage vector diagram of the 5-level single-phase converter, as it is shown in Fig. 2, for each sector, a predefined vector sequence is considered. The predefined vector sequences are listed in Table 3. In addition, the applied times of different vectors (t_x, t_y) are shown in Fig. 2. It is worth mentioning that both available small vectors are employed with adjustable time duration (t_{y1}, t_{y2}) in each switching sequence to control the NP voltage.

In this MPC algorithm, the cost function is defined as follows [17]:

$$CF(n) = \left| v_d(n+1)^* - v_{ab}(n) \right| \tag{9}$$

where $v_d(\mathrm{n}+1)^*$ is the reference waveform and $v_{ab}(\mathrm{n})$ is the output voltage vector of the converter. Considering (9), the value of the cost function for small vectors of each sector is the same. These values are described as follows:

$$\begin{cases} CF_2(n) = CF_3(n) \\ CF_6(n) = CF_7(n) \end{cases} \tag{10}$$

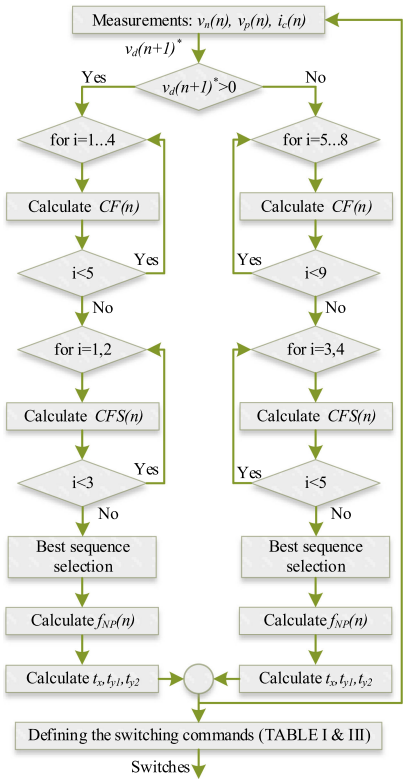

FIGURE 4. The flowchart of the MPC with constant switching frequency.

The reference voltage can be applied through the vector sequence with a defined time duration as follows:

$$\begin{cases} v_{ref} T_s = v_x t_x + v_y t_y \\ T_s = t_x + t_y \end{cases} \tag{11}$$

where $v_{ref} = v_d(n+1)^*$, v_x and v_y are the voltage vectors related to the considered vector sequences for each sector.

According to (11) the applied time duration of vectors can be calculated. For example, v_x is set to be the full dc-link voltage vector (P), and v_y will be the small vectors of HP^{+} and HP^{-} in sector I. Moreover, t_y is divided between small vectors. Thus, the applied time of each vector is derived as follows:

$$\begin{cases} t_x = T_s(1/CF_x(n))/((1/CF_x(n)) + (1/CF_y(n))) \\ t_y = T_s(1/CF_y(n))/((1/CF_x(n)) + (1/CF_y(n))) \\ t_y = t_{y1} + t_{y2} \end{cases} \tag{12}$$

where t_{y1} and t_{y2} are the applied times of the first and second applied small vectors for each sector as it is described in Table 3.

To find the best vector sequence, another cost function is defined for each sector as (13) [17].

$$CFS(n) = CF_x(n)(t_x/T_s) + CF_y(n)(t_y/T_s) \tag{13}$$

Therefore, the sector cost function with minimum value will be selected, and related execution times are applied.

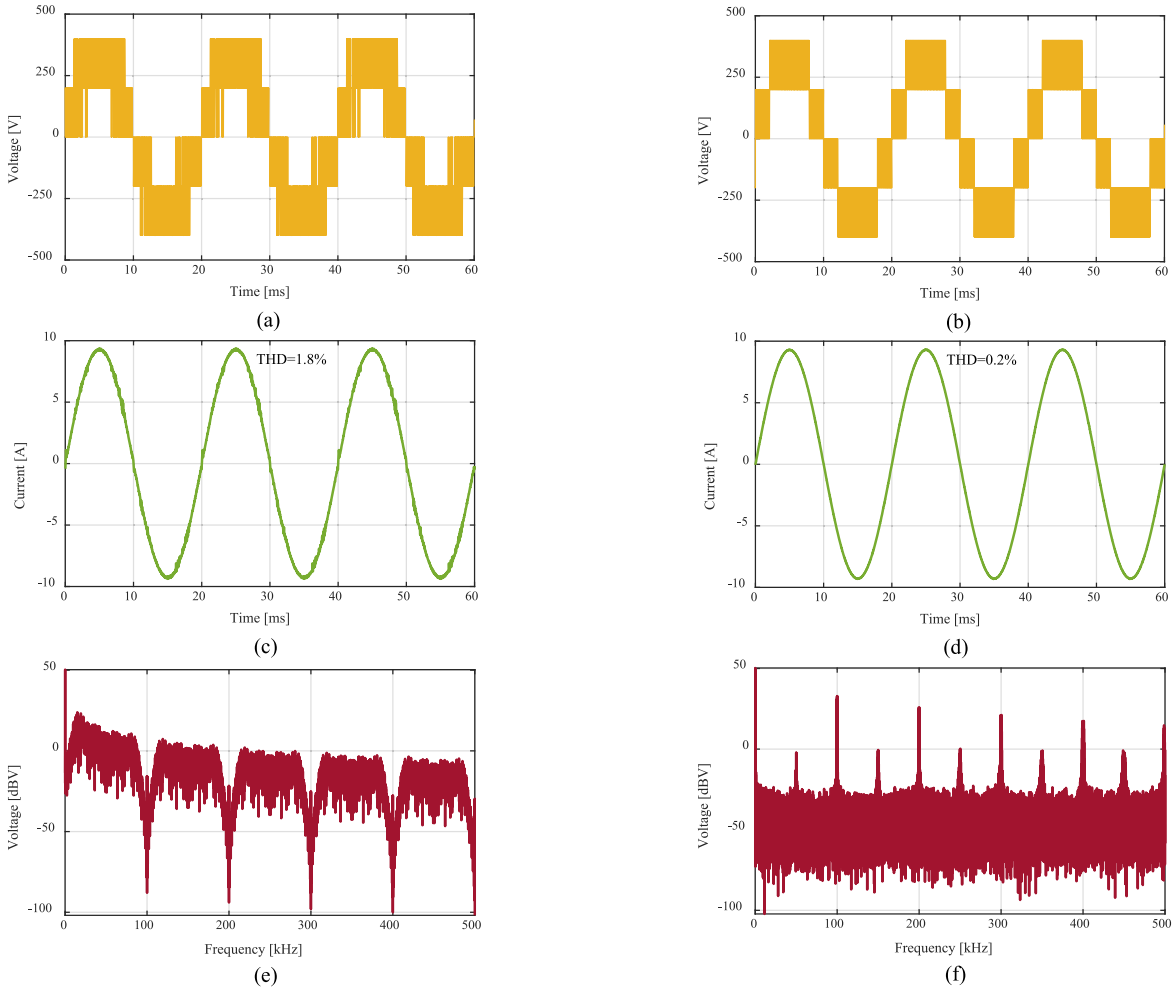

FIGURE 5. The simulation results (a) output voltage of the converter of adopted MPC, (b) output voltage of the converter of MPC with constant switching frequency, (c) load current of adopted MPC, (d) load current of MPC with constant switching frequency, (e) the FFT result of the output voltage of the converter for adopted MPC, (f) the FFT result of the output voltage of the converter for MPC with constant switching frequency.

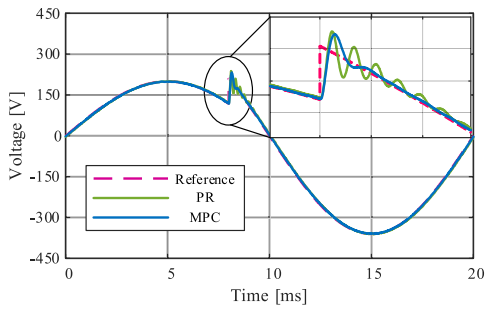

FIGURE 6. Simulation results of the reference voltage step change for PR controller with carrier-based modulation and MPC with constant switching frequency.

Compared to [17], to control the NP voltage, another function with consideration of output current is defined as follows:

$$f_{NP}(n) = \lambda(v_p - v_n) \times sign(i_c)/V_{DC} \tag{14}$$

where λ is a weighting factor in regulating the NP voltage.

Based on the voltage difference of upper and lower dc-link capacitors, the applied time duration of the small vector for each sector will be modified as (15) to keep the NP voltage constant.

$$\begin{cases} t_{y1} = (1 + f_{NP})t_y \\ t_{y2} = (1 - f_{NP})t_y \end{cases} \tag{15}$$

The flowchart of the proposed MPC with constant switching frequency is shown in Fig. 4, which is divided into two sections based on the value of the reference voltage. In each section, three cost functions of (9), (13) and (14) are calculated. For example, when the reference voltage is positive, first the cost functions of four positive output voltage vectors (V_1, V_2, V_3 and V_4) are calculated based on (9). After that, the cost function of the two positive sequences of I and II are determined by using (12) and (13). The sequence with a lower value of CFS is selected through the best sequence selection function in the flowchart. After that, the cost function of NP voltage balancing of (14) is determined, and consequently, the applied time duration of each vector is calculated through

TABLE 4. The System Parameters

Parameter	Definition	value
V_{DC}	dc supply voltage	400 V
V_d	The voltage across the load	230 V (rms)
C_p, C_n	dc-link capacitors	1 mF
L_c	Filter inductance (MPC with constant switching frequency)	600 µH
	Filter inductance (adopted MPC)	1.2 mH
R_c	The resistance of filter inductor	0.1 Ω
C_d	Filter capacitor	2 µF
R	Load resistance	35 Ω
f_{sw}	Switching frequency (MPC with constant switching frequency)	50 kHz
f	Reference output frequency	50 Hz
T_s	Sampling time	10 µs

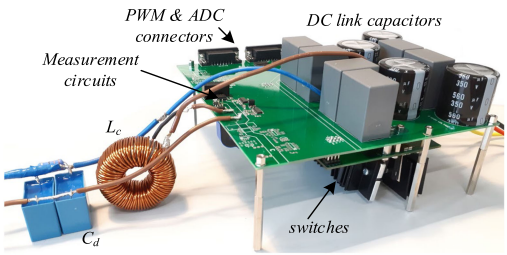

FIGURE 7. The 5-level single phase hybrid ANPC inverter with an LC filter.

(15). Finally, the switches commands are determined in the last function.

IV. RESULTS

A. SIMULATION RESULTS

In order to verify the ability of employed MPCs, two simulations for both the MPC algorithms are performed. The parameters of the system are listed in Table 4. The simulation results are shown in Fig. 5. Fig. 5(a) and (b) show the output voltage of the converter for adopted MPC and MPC with constant switching frequency. By comparing Fig. 5(a) and (b), it can be seen that there are fewer transitions between sectors when the MPC with constant switching frequency is applied. However, when adopted MPC is utilized, there are many transitions between sector 1 and sector 2 or sector 3 and 4. These transitions increase the current distortion and consequently increase the THD of the output current. This fact is shown in Fig. 5(c), (d), wherein the THD of current for constant switching is less than 1%.

Moreover, the Fast Fourier Transform (FFT) results of output voltage for both MPC are depicted in Fig. 5(e) and (f). Fig. 5(e) is related to the adopted MPC. As can be seen, the harmonics are spread in a wide range of frequencies. This leads to using a bulkier output filter. Fig. 5(f) shows the FFT result of MPC with constant switching frequency. Since both small vectors are employed in each switching cycle, the first major harmonics appear at twice the switching frequency (100 kHz). Thus, the filter is designed based on this frequency,

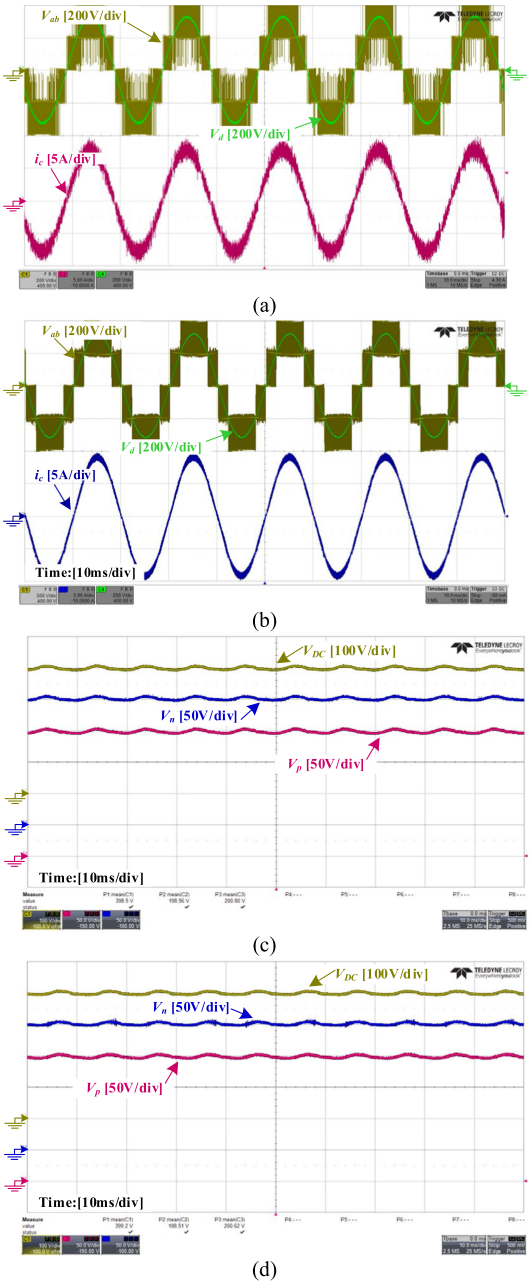

FIGURE 8. Experimental results (a) the output voltage of the converter, the load voltage and the current of filter inductor for adopted MPC, (b) the output voltage of the converter, the load voltage and the current of filter inductor for MPC with constant switching frequency, (c) the voltages of dc-link and dc-link capacitors for adopted MPC, (d) the voltages of dc-link and dc-link capacitors for MPC with constant switching frequency.

in which the filter inductor is roughly 50% smaller than other MPC. In addition, Considering the sampling time of 10 µs, the maximum switching frequency at the output voltage of the converter can be 50 kHz for the adopted MPC. Therefore, the equivalent switching frequencies of the presented methods are not equal.

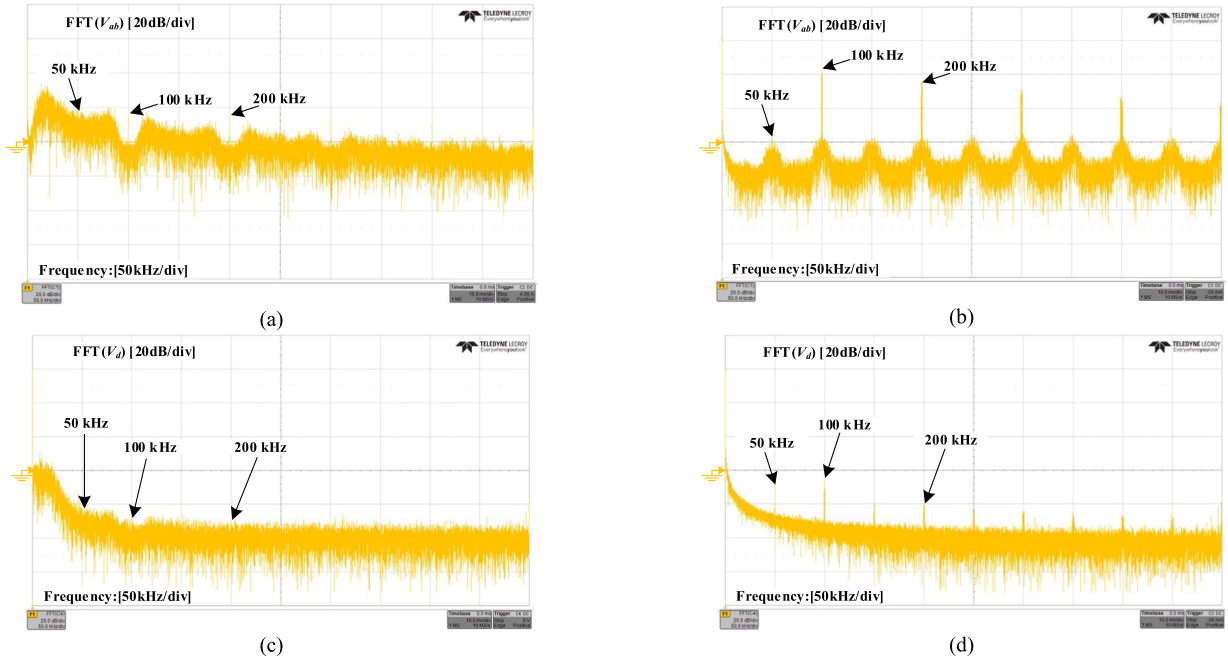

FIGURE 9. The FFT results of (a) the output voltage of the converter for adopted MPC, (b) the output voltage of the converter for MPC with constant switching frequency, (c) the voltage across the load for adopted MPC, (d) the voltage across the load for MPC with constant switching frequency.

By comparing the results of both MPC, it can be recognized that the MPC with constant switching frequency shows a better behavior in terms of converter current ripple and THD of the output voltage. Moreover, based on the FFT results, an LC filter with a higher cutoff frequency is required for MPC with constant switching frequency.

To show the behavior of the controller during transitions, a simulation is carried out for the MPC with the constant switching frequency and a traditional control scheme with a carrier-based modulator. In a traditional control scheme, a voltage control loop with a PR controller is designed to regulate the output voltage (voltage across the load), in which the PR controller provides a reference waveform for a modulator. In addition, the carrier-based modulation technique of [31], [32] is modified to control the NP voltage. The same simulation parameters are employed for both methods. In this simulation, the reference voltage is changed and the transient responses of two systems are captured, as are shown in Fig. 6. As it can be seen, both controllers follow the reference voltage with fast response; meanwhile, the MPC with constants switching frequency reaches to steady state shortly after the transition. However, for the PR controller, it takes a longer time to pass the transition.

B. EXPERIMENTAL RESULTS

The prototype of the converter with the designed filter is shown in Fig. 7, where SiC and Si MOSFETs are employed. The considered MPCs are implemented with the dSPACE's Micro-Lab Box ds1202, which the control part is carried out in dSPACE's microprocessor. Meanwhile, the FPGA is utilized to implement the switching sequences with consideration of the deadtime of devices. A dc-voltage supply (EA-PSI 81000-30) is used to regulate the dc-link voltage at 400 V.

The steady-state results for both MPCs are shown in Fig. 8. The output voltage of the converter, the current of the filter inductor, and the voltage across the load are shown in Fig. 8(a) and (b). As can be seen, the current ripple at adopted MPC is higher even though a bigger inductor is utilized. The voltages of dc-link capacitors are shown in Fig. 8(c) and (d). As can be seen, these voltages are regulated at the same level, which equals 200 V. Moreover, the peak-to-peak ripple voltage of dc-link is 23 V, which is 5.7 percent of dc-link voltage (400 V).

The FFT result of the output voltages are shown in Fig. 9(a) and (b). For the MPC with the constant switching frequency, the major harmonic appears at 100 kHz, which is two times larger than the switching frequency. As mentioned before, the reason is that both two small vectors are utilized in each sector. Due to the difference in the applied time of small vectors, the odd multiple harmonics of switching frequency are presented in the output voltage with less amplitude than even ones. However, for the adopted MPC, the harmonics spread in the whole frequency range. Moreover, The FFT results of the voltage across the load for both methods are shown in Fig. 9(c) and (d). As can be seen, the filter reduces the amplitude of output voltage harmonics.

To verify the performance of the implemented MPC regarding the NP voltage balancing, an experiment is done for MPC with constant switching frequency. In this experiment, a load is added in parallel with the lower dc-link capacitor and a relay is utilized to connect and disconnect the load. The converter schematic with added load is shown in Fig. 10(a). Fig. 10(b) shows the dc-link capacitor voltages and the current

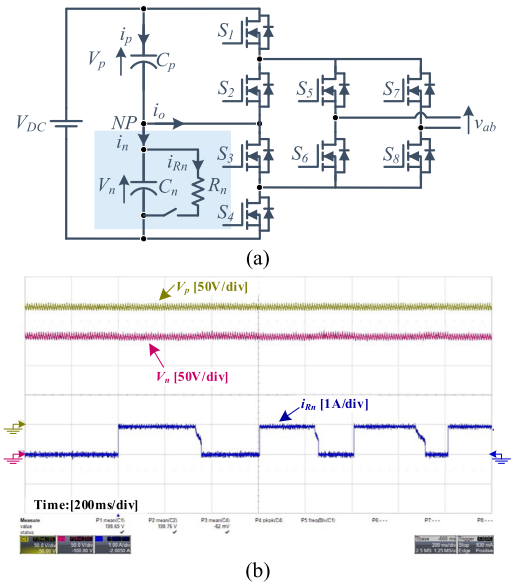

FIGURE 10. Experimental results (a) the placement of the added resistor in parallel with the lower dc-link capacitor, (b) the voltages of dc-link capacitors and the current of resistor in parallel with the lower dc-link capacitor.

of the added load. As it can be seen, despite connecting and disconnecting the load, still the voltage of the lower dc-link capacitor is regulated and fixed at the same level as an upper dc-link capacitor voltage.

V. CONCLUSION

In this paper, two different high bandwidth MPCs, including adapted MPC and MPC with the constant switching frequency, were developed for a high switching frequency single-phase 5-level hybrid ANPC inverter. Wherein SiC MOSFETs are employed to increase the switching frequency and to reduce the size of the filter. To control the NP voltage, the effect of each output voltage vector was studied. Moreover, a sub-cost function was applied to regulate the NP voltage. Both the methods were experimentally investigated by a laboratory setup. The simulation and experimental results show the ability of methods to control the voltage across the load and to balance the dc-link capacitor voltages during both steady-state and transitions. Comparing both methods showed the MPC with constant switching frequency has more advantages, such as better harmonic spectrum distribution and smaller filter size due to locating the main harmonics around twice the switching frequency.

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