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Using OPNET to Model and Evaluate the MU Performance Based on IEC 61850-9-2LE

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Abstract

The growth of IEC61850-9-2 process bus as a high data rate communication network have a great improved the capability of substation automation system (SAS). This paper discuss a modelling concept of intelligent electronic devices (IED) using OPNET modeller simulation tool. Simulation tool provides a comprehensive development environment for the specification modelling, system simulation and also facilitate performance evaluation of the system under study with different topologies that guide the SAS network engineers based on planning and design. Several testing has been made based on the modelled merging unit (MU) IED within two scenarios. The behaviour of the Ethernet switches with the sampled value (SV) traffic stream has been discussed within the first scenario. It shows that the first Ethernet switch experienced more latency than the subsequent switches based on it serialized the bunched SV frames whereas the subsequent switches experienced less latency in which that may facilitate the design of the large SAS that consist more than one Ethernet switch to reduce the cabling between switchyard and control station. SV traffic stream latencies have been evaluated to assess the limits and capacity of the process bus network critical components and shows that the overall of the 19 MUs latency is within the acceptable latency range (250 μs). However based on adding MUs 20-23 the latency has been increased significantly within scenario two.
Keywords: IEC61850-9-2LE; processbus; OPNET; substation Automation system (SAS); modeling

Nomenclature

SAS   Substation automation system
IED   Intelligent electronic devices
MU   Merging Unit
SV   Sampled Value
DES   discrete event simulation
LAN   local area network
ETE   end-to-end
GOOSE General Object Oriented Substation Events
CUT   Coordinate Universal Time
SNTP   Simple Network Time Protocol
IRIG-B Inter-Range Instrumentation Group time code B
FSM   finite state machine
STD   state transition diagram
QoS   quality of services

1. Introduction

The wide internationally acceptance of the IEC 61850 standard and the growth of IEC 61850-9-2 process bus as a high data rate communication network has a great improvement to the capability of SAS. IEC 61850-9-2 provides distributed measurements for monitoring, control and protection functions [1]. In both industry and academia engineers attempt to establish and test the new approaches, taking the advantages of the PC-based technology to build individual test situation based on modelling and simulating the system components. However, there are several another feasible system performance evaluation methods such as analysis, mathematical modeling, Test-bed emulating and hybrid simulation. These methods have several advantages and disadvantages, for instance analysis and mathematical modeling however it can provide fast answering for the problem that have being studied but in general many of the cases are inapplicable and lack accuracy through the approximation process. Moreover, it cannot reflect the real behavior of the system especially when its related to the communication network issues such as queues and protocols in which that can be decomposed or approximated by reducing the studied model to a typical model to reduce the analytical difficulties. Whereas, Test-bed based on operation point view involves implementing the studied case into the real-word hardware in a much smaller scale size in which that still suffering from the other real word difficulties that may completely irrelevant to the studied cases. Also the cost may be significant and not suitable for analyzing large system [2].

As regard system simulation provides a way to model the system behavior and analyze the interaction among the system modeling components by using the discrete event simulation (DES). DES has been considered as the typical method in large-scale simulation studies that provides modeling and solution in a more accurate and realistic way, since it reflects the real behavior of the system under studies by creating an extremely system network details, packet-by-packet model for the events within the network under studies.

With this motivation, this paper takes the simulation approach to determine and predict the real behavior of the process bus network by using Optimized Network Engineering Tool OPNET which is more suitable for the development engineers rather than end users. OPNET provides a comprehensive development environment for the specification modeling, simulation and performance analysis for the system under study. A wide scale of communication systems from a single local area network (LAN) to global satellite networks with different communication technologies that able to support.

The methodology presented in this paper within the first step provides the modelling of the MU which is an IEC 61850-9-2LE compliant device that publishes digital measuring signals such as current and voltage from primary SAS components current and voltage transformers (CTs and PTs) to bay controllers and protection relays in station

layer. MU is an interface between existing analog primary SAS components and the new command, control and protection digital IEDs based on the IEC 61850-9-2LE for building digital bays or full digital substations. It also allows there placement of expensive copper cables by optical fibres. In the second step a series of test for the process bus network under different circumstances based on different scenarios are implemented. These scenarios are used to illustrate and to determine the real behavior of the process bus network based on calculating the latency of the SV traffic stream between the publishers and the subscribers. The SV latencies have been considered as a unique critical characteristic that have a hard real time requirement and can be increased and decreased based on changing of the network topology and traffic within the network under test.

Significant growth within the process bus network based on product development and several process bus SAS have been commissioned. However, regardless to this growth the knowledge about the real behaviour of the process bus network, especially when there is a large number of traffic resources are connected within the same network is little. The process bus network analysis is in the focus of research area from both industrial and academia, several network process bus modelling have been under testing, however their hard assumption limit   their effectiveness [3]. In [4] modelling and simulation of the distribution substation 69 kV and 220 kV, however the raw data of the SV traffic characteristic that been used is uncompliant with IEC 61850-9-2LE. Where as in [5] several works have been done based on test bench that calculate and compare the characteristic of the SV traffic differences between the two baths direct from merging unit and the source of the digital reference signal. David Ingram has been done several works that discussed the proses bus critical issues such as time synchronization, routing and process bus traffic analysis. Most of the work had been done by using the GTNET card with the SV firmware to generate the MU stream and the Endace DAG7.5G4 network card to monitor the traffic. The weak points of those works they cannot reflect the real behaviour of the system since the generated streaming traffic was based on mathematical calculation (number of MU within the network multiply by the traffic that each MU can generate in every second) and then injected the traffic to network. According to injected traffic calculation of the behaviour for the rest of the network component had been done [6], [7].

The strongest points of this work are every node within the process bus network has been modelled by using OPNET in which that simulates the real physical SAS components. Moreover, the traffic that has been generated by every node is complaint with the IEC 61850-9-2LE standard and the interaction between those nodes is reflects the real behaviour of the SAS, since every node has been connected to the communication network one by one. Furthermore, the interactions between connected nodes have been monitored based on measuring end-to-end (ETE) latencies from the publisher and subscriber nodes point view.

2. System architecture and interfaces

The functions in substation automation are implemented according to the standardized data model which can be divided into three different levels based on the substation architecture. Fig. 1 (a) illustrates the three levels as station, bay and process level functions besides the associated logical interface numbers. In the bottom is the process level which links with the bay level by interfaces number four and five. Based on these interfaces it is able to exchange control commands and information data.

Usually, primary apparatuses such as circuit breakers, transformers, switchgears etc. are located in process level. The level may also have IEDs such as intelligent sensors and actuators. The input and output messages of these apparatuses are basically consisting of information such as the transformer voltage and current values as an analogue signal format, and control commands from the bay relays as a binary signal format. Data gathering starts at the process bus level with instruments transformer (IT).
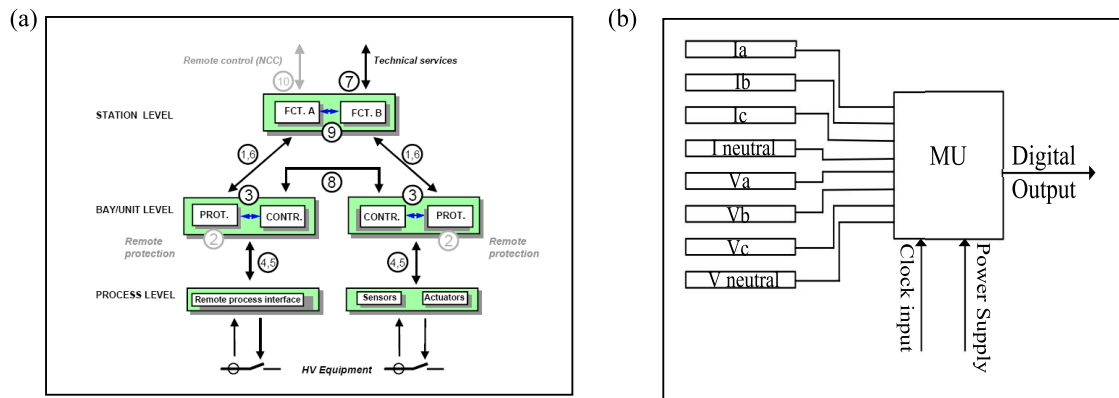
Fig. 1. (a) Levels and logical interface IEC 61850; (b) MU concept.

The analogue data signal is converted into digitalized standard packets by so-called Merging Unit (MU) for subsequent transmission through the process bus LAN. It may locate in the yard or it can be integrated with the instrument transformer. MU can transmit over the point-to-point type connection to any IED or broadcast over the LAN in the similar manner as GOOSE messages. Process bus data is denoted with number 4 and 5 interfaces [8]. Process bus also used to control high voltage equipment such as breakers, breaker control units, disconnected switches etc. Process level digital information is then communicated over the LAN to the protection and control devices that are located at the Bay level. Process bus approach promises to reduce the installation cost by significantly reducing the copper wires and replacing it with the logical connection [1]. According to the proposed process bus solution architecture MU has the ability to connect the analog word to the digital word within the SAS as illustrate in Fig. 1(b) that introduced another critical components to the power system such as Time synchronization source and Ethernet switch [10],[11]. According to the IEC 61850-9-2 that specified how SV measurements can be transmitted over the LAN whereas IEC 61850-9-2LE (Light Edition) reduces the complexity and difficulty of implementation associated within the first version [9]. This improvement has been achieved by restricting the data sets that are transmitted and specifying the sampling rates. The assigned dataset comprises four voltages and currents three phases and neutral for each as illustrated in Fig.1.

3. OPNET modelling methodology

In order to build a simulation model that can produce results within an acceptable timeframe the real-life system network must be simplified. The simplification of the real-life system network can be made based on the simulation goals that had been identified previously. The simulation goals are to examine and predict the real behavior of the system under test with respect to different parameters such as mean delay, delay variations, traffic lost, traffic drooped, error, etc. As regard in this paper OPNET has been used to model the IEC 61850-9-2 process bus network in a simplified way that different SAS components have been modeled and connected within several scenarios using OPNET modeling tools. OPNET provides several editors that facilitate and simplifying the modeling task. In this part description for the most commonly used editors has been overviewed. These editors are organized in a hierarchical manner from down to up parameter editor, process editor, node editor and project editor. The parameter (include packet format editor) editor is always considered as a utility editor rather than modeling domains that the user could configure the modeled node parameters and traffic generation parameters such as MAC address, destination address, start time, stop time, inter-arrival time, packet size, etc. While OPNET process model editor is used to describe the logic flow and behavior of processors, protocols, resources, application, algorithms and queues modules using finite state machine (FSM) approach. Process model consists of state and state transition diagram (STD) that expressed in language called Proto-C with an extensive library of kernel procedure, and the standard C programing language. The states and transitions graphically describe the progression of a process in response to to

events. Within each state, general logic can be specified by implementing the predefined library and even the full flexibility of the C language or linking to an external program. Fig. 2(a) illustrates process model for the traffic generation source module for the MU.

Node editor has been considered as a user interface tool in which that a user can model a physical device and edit the internal structure of the modeled device or node. Node model is consists from several modules that separated by logical functionalities.

(a)   (b)   (c)
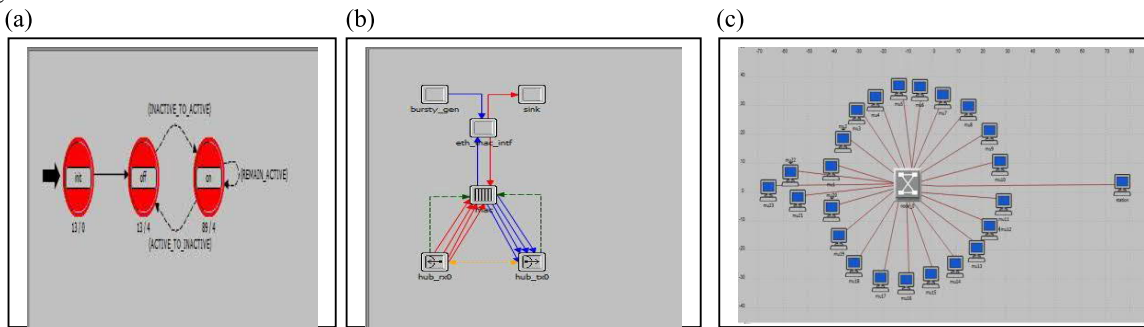

Fig. 2. (a) OPNET process model; (b) OPNET node model; (c) OPNET project model

These modules are interconnected by packet stream or statistic wires. Each particular node function can be represented by a particular module in which that modules can be used to transmit packet, receive packet, process data, store data, route packets, etc. Fig. 2(b) illustrates the modeled MU IED node model diagram that can be used within the process bus network to simulate the the SAS. Where the Ethernet MAC node model provided with OPNET nodes model library implements the carrier sense multiple access collision detection CSMA/CD and retransmission mechanisms specified in the IEEE 802.3, IEEE 802.3z standard [12]. Within the Ethernet MAC model the following features provided serialization of bit transfers to and from the physical layer, first input first output (FIFO) processing of transmission request, propagation delay based on the distance between connected nodes, carrier sensing and collision detection within the physical layer and support full-and half-duplex transmission. Ethernet MAC node models have been used within this work process bus network test models.

Project editor is used to specify the system topology of communication network that may be considered as the one that may use for for every simulation task. Within the project editor user can define the position and the interconnection of the modeled nodes that the system consists from. The network of the modeled system can be complex since the project editor can support different kind of nodes such as fixed, mobile and satellite. However the complexity can be eliminated by implanting the subnetwork approach that can be arraigned in hierarchical manner. In subnetwork lower level that may only consists from nodes and communication links. Project editor can grouped all those subnetworks where communication links facilitate communication between those subnetworks. Fig. 2(c) illustrates the MU IED nodes in the SAS [2], [12].

4. Case study

MU reliability and proper functionality plays major role within the SAS. For instant incorrect measurements, delays and errors may lead to incorrect resolution of a protective and control IEDs that may cause in serious damage. Therefore within this part the SV traffic stream latency have been evaluated. The purpose of these evaluations and testing are to assess the limits and capacity of the process bus network critical components such the communication links, Ethernet switch number that the SV traffic stream may pass to reach their destination with the associated latency experience when passing these number of Ethernet switches and the number of MU that may composed in a single process bus network are the focus of this study based on two scenarios.

In the first scenario and within the first step MU has been modeled as a SV messages publisher and receiving IED has been modeled to subscribe to the publishing MU SV traffic stream as illustrated in Fig. 3(a) These nodes (MU and IED) have been used in both scenarios. Numbers of Ethernet switches have been used one by one in series to connect the MU with the receiving IED. Calculation of the SV traffic stream ETE latency associated with adding

switch that may the SV traffic experienced based on different LAN speed 10Mb/s and 100Mb/s. It is worth noticing that all nodes for both scenarios are synchronous based on the assigned simulation start time and stop time. MU SV traffic stream has been created based on the IEC 61850-9-2LE that the MU can send 4000 packet per second as the sampling period (50 Hz and 80samples/c) and the packet size 126 byte plus header. This SV traffic was created within the custom MU modeled node in which that allows SV traffic key parameters to be assigned specifically. Priority tagging has not been considered since there is no another traffic within the simulated process bus network. Moreover according to the modeled Ethernet switch quality of services (QoS) parameters it has one queue with a packet service rate 100000 packets/s. This scenario present and simulate the approach of large SAS when the messages pass more than one switch to reach their destination. Fig. 3(b) illustrates the latency for five configuration start from the latency of the SV traffic stream (bunched frames) have passed through single Ethernet switch within the 10 Mb/s LAN to the fifth Ethernet switches. Within the first configuration which is the single Ethernet switch the latency was 245,534992 μs whereas every Ethernet switch add almost fixed amount of latency 110-120 μs.
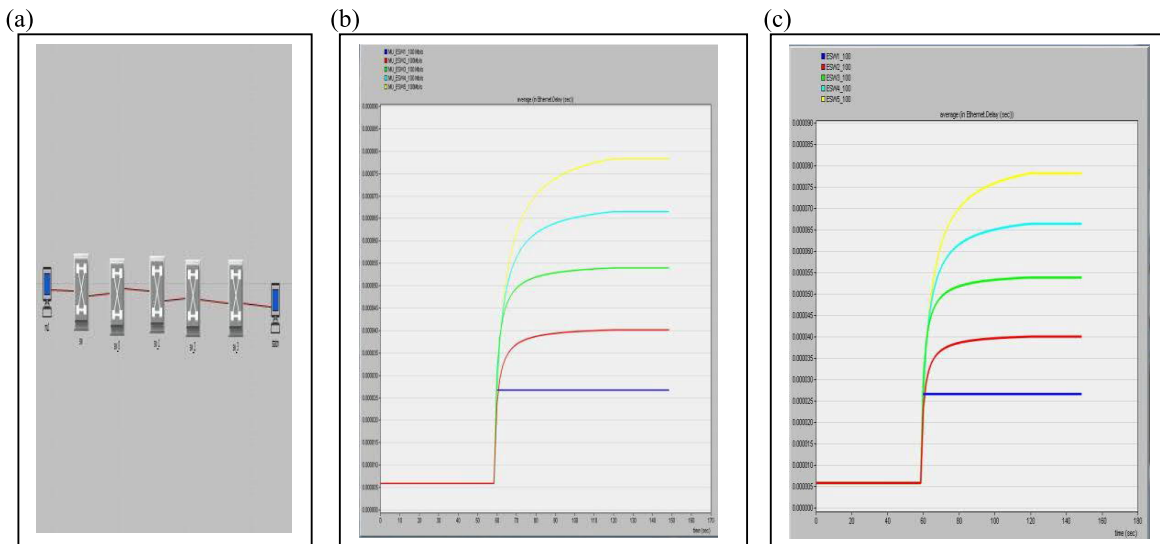

Fig. 3. (a) MU sv traffic stream; (b) sv Traffic stream average latencies LAN 10Mb/s; (c) sv Traffic stream average latency LAN 100Mb/s

This result has been considered as significant results since the first Ethernet switch experienced more latency than the subsequent switches based on it serialized the bunched SV frames whereas the subsequent switches experienced less latency in which that can be used to connect large SAS efficiently without significantly increasing the overall latencies of the SV traffic stream. Therefore according to Fig. 3(b) last Ethernet switch experienced latency was 693.8105 μs. Fig. 3(c) illustrate the latency for five configuration start from the latency of the SV traffic stream (bunched frames) have passed through single Ethernet switch within the 100 Mb/s LAN to the fifth Ethernet switches. The latency that the SV traffic stream has experienced when pausing the first switch was 2.6654 μs whereas every Ethernet switch add almost fixed amount of latency 11-13 μs.

According to Fig. 3(c) last Ethernet switch experienced latency was 78,274175 μs. Within the second scenario several modeled MU have been connected to the process bus network by increasing the number of MU by one each time. The purpose of these tests is to evaluate the limits of capacity of the process bus network critical components such the communication links and the Ethernet switch. In the first step where the LAN speed 10Mb/s the first MU has been connected within the process bus network. 60000 packets have been created based on 15 seconds traffic generation where the SV traffic stream latency was 250.5581 μs.
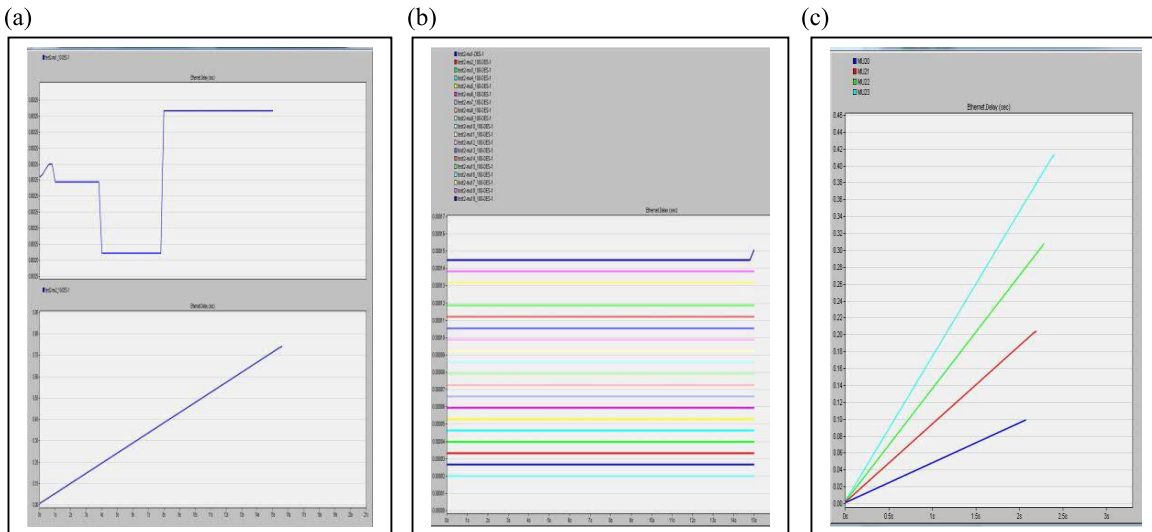
Fig. 4. (a) SV average latency LAN 10Mb/s; (b) SV average latency LAN 100Mb/s; SV average latency LAN 100Mb/s

This SV traffic stream latency is within the acceptable range since the maximum latency when there is no packet loss is expected to be 250 µs whereas by connecting two MUs the SV traffic stream latency has been increased to 0.72237s in 15 seconds linearly as illustrated in Fig. 4(a) The theoretical throughput that every MU can create is 4.418 Mb/s with a 50 Hz, 80sample/c and 126 frame plus header.

In the second scenario where the LAN speed 100Mb/s several modulated MUs have been connected to the process bus network. Each test the number of the MUs within the process bus network increases by one. This test reflect the real behavior of the process bus network when the SV traffic stream increase based on increasing the the number of MU within the network. Moreover it shows the capacity of the process bus network based on the speed of the LAN network and also the process bus tolerance based on the limitation of the number of MUs that have to be connected within the SAS as the configuration illustrated in Fig. 2(c) Every MU generates SV traffic stream 4000 packet/s as a result 19 Mu units generate 1140000 packets within 15 seconds. From Fig. 4(b) the first MU latency was 26,6613 µs whereas every MU add almost fixed amount of latency to the SV traffic stream ≈ 6 µs. Also the 19 MU add latency to SV traffic was 144,914583 µs which is within the acceptable latency range 250 µs. However based on adding MUs 20-23 the latency has been increased significantly as illustrated in Fig. 4(c) and Table 1 where it is not acceptable based on the SV limitation (SV traffic stream without error 250 µs).

Table 1. An example of a table.

	MU20	MU21	MU22	MU23
T(s)	0.0958	0.1960	0.2712	0.3629

These latencies have been recognized and defined that they occur based on reaching of the limits of the LAN speed 100Mb/s, whereas the Ethernet switch still operating in a normal way without packet dropping (23 MUs generate 184004 packets within 2 seconds, station sink destroy 184.002 packets: OPNET statistic) since it can serve packets based on processing rate 100000 packets/s. The Ethernet queue size is 100 packets.

5. Conclusion

In future mixed buses (process bus, station bus) promise to be seen within the SAS network since the process bus shows more reliability and flexibility for the high data rate network traffic. This can be achieved by utilizing the modern technologies and network components such as IEDs, links and Ethernet switches. In this paper modeling of the modern IEDs have been discussed to build SAS process bus network and evaluate the performance of the simulated network under different circumstances using OPNET. OPNET has been shown as an efficient tool for modeling and solving critical performance issues within SAS network. Through the simulation of the process bus network the unique characteristic of the SV networks that have a hard real time requirement have been modeled and evaluated. Measurements from modeled IEDs and several process bus network have been confirmed that the first Ethernet switch experienced more latency than the subsequent switches based on it serialized the bunched SV frames whereas the subsequent switches experienced less latency in which that can be used to connect large SAS efficiently without significantly increasing the overall latencies of the SV traffic stream. Latencies have measured based on connecting several MUs within a process bus network to evaluate the limits of capacity of the process bus network critical components such the communication links and the Ethernet switch in which that may facilitate the design and guide the engineers to build the SAS in efficient way and also shows that the overall of the 19 MUs latency is within the acceptable latency range (250 μs). However based on adding MUs 20-23 the latency has been increased significantly within scenario two.

Acknowledgements

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